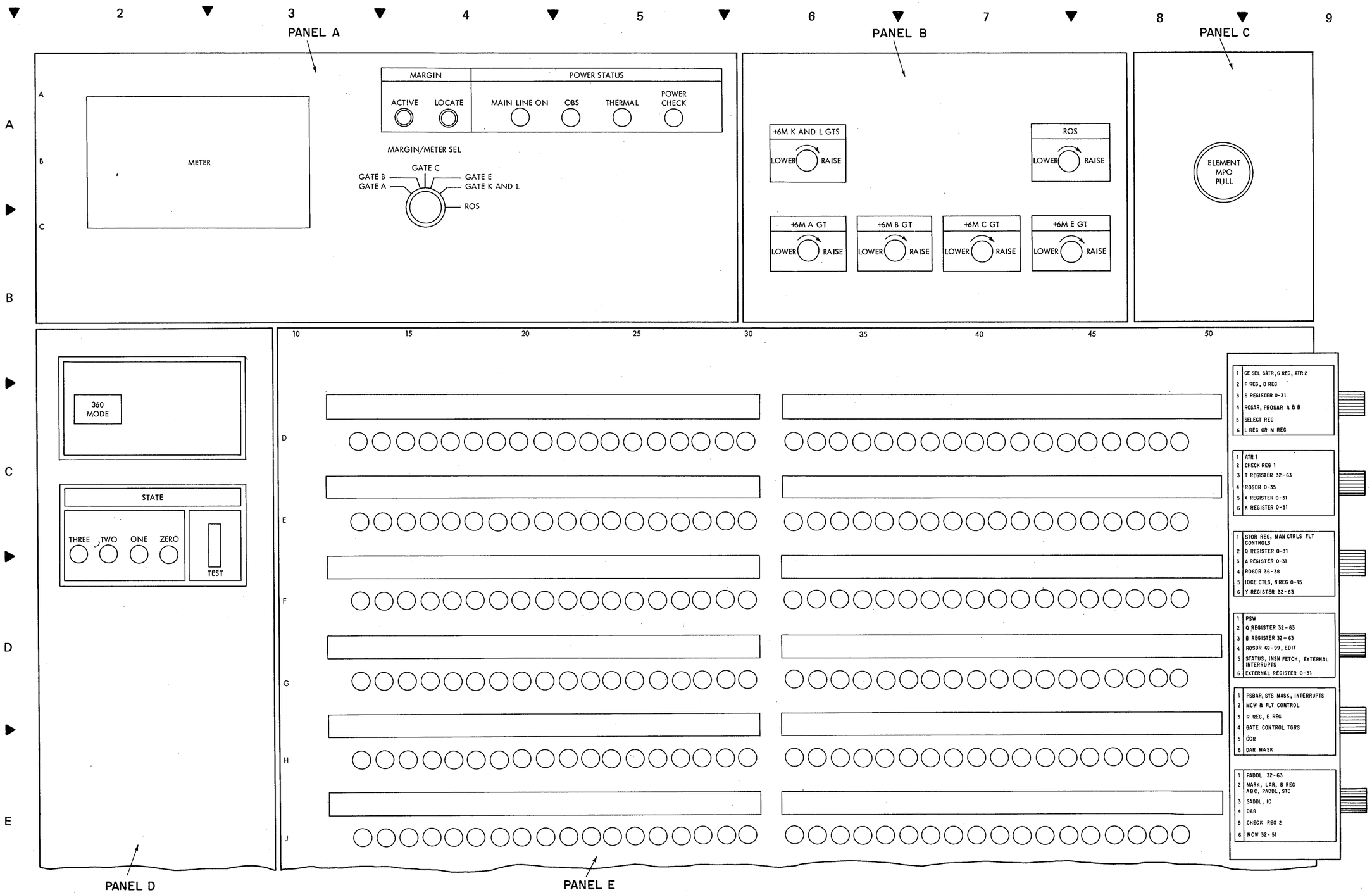


Diagram 6-1. CE Control Panel (Sheet 1 of 2)

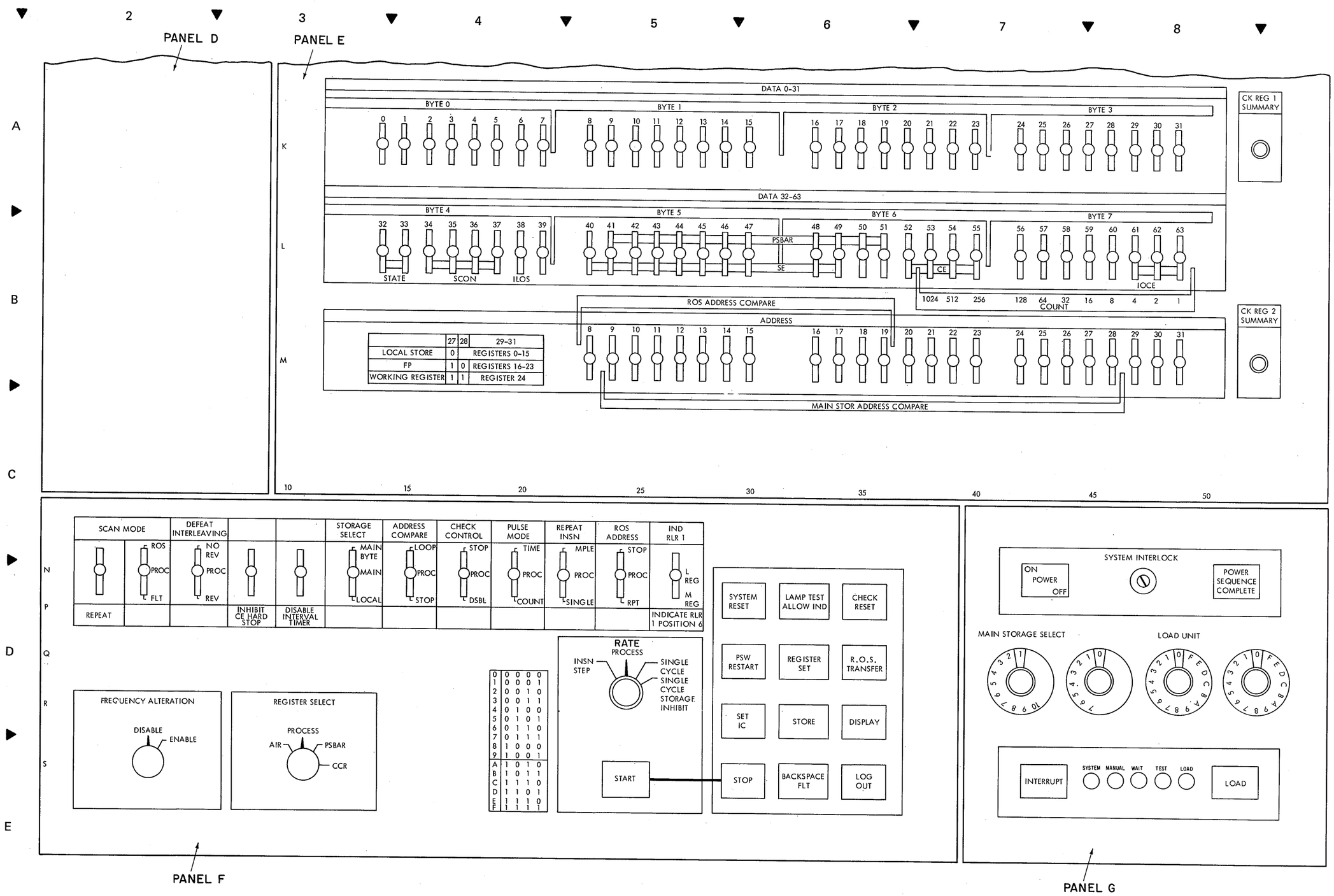


Diagram 6-1. CE Control Panel (Sheet 2 of 2)

DISPLAY NO. 1

Roller Pos.	Indicators
1	CE SEL ATR: 1, 2, 3, 4 · T C STEP · G REGISTER (WRITE DIRECT): P 0-7, 0, 1, 2, 3, 4, 5, 6, 7 · ATR-2: P 32-39, 32, 33, 34, 35, 36, 37, 38, 39
2	F REGISTER (READ DIRECT): P 0-7, 0–7, P 8-15, 8–15 · D REGISTER: P 16-23, 16–23, P 24-31, 24–31
3	S REGISTER: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31
4	READ ONLY STORAGE ADDRESS REGISTER: 0–11 · ROS PREVIOUS ADDRESS REGISTER A: 0–11 · ROS PREVIOUS ADDRESS REGISTER B: 0–11
5	SELECT REGISTER: P 0-7 · PAM/RCU: 1, 2, 3 · TCU: 1, 2, 3 · P 8-15 · SE: 1, 2, 3, 4, 5, 6, 7 · SE/DE 8 · P 16-23, 9, 10 · CE: 1, 2, 3, 4 · P 24-31 · IOCE: 1, 2, 3
6*	L REGISTER: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31
6*	M REGISTER: P 32-39, 32–39, P 40-47, 40–47, P 48-55, 48–55, P 56-68, 56–63

DISPLAY 1	
1	CE SEL SATR, G REG, ATR-2
2	F REG, D REG
3	S REG (0-31)
4	ROSAR, PROSAR A AND B
5	SELECT REG
6	L REG*
6	M REG*

*Selected via INDICATE ON ROLLER 1 POSITION 6 switch.

DISPLAY NO. 2

Roller Pos.	Indicators
1	ADDRESS TRANSLATION REGISTER 1: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31
2	E REG PTY · PADD FULL SUM: 4-7, 8-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-63, 64-67 · MLPR DECODE PTY · PADD HALF-SUM: 4-7, 8-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-67 · ERROR TGR · ROS PTY: 2-42, 43-68, 69-99 · SADD: HALF SUM, FULL SUM
3	T REGISTER: P 32-39, 32–39, P 40-47, 40–47, P 48-55, 48–55, P 56-63, 56–63
4	0, 1 · W FAA CONTROLS: 2, 3, 4, 5 · A AB, IC INGATES: 6, 7, 8, 9 · B LS-T 10, LS-S 11 · C ST, D, Q, G, PSW INGATES: 12, 13, 14, 15, 16 · D FLT 17 · F INGT AND EOP: A FIELD 18, SD 19, P 6-42 · E EMIT E, R INGATES: 21, 22, 23, 24 · F MISC CONTROL PART 2 FLT B FIELD: 25, 26, 27, 28, 29, SF 30 · G MISC CONTROL PART 1 FLT C FIELD: 31, 32, 33, 34, SG 35
5	X REGISTER: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31
6	K REGISTER: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31

DISPLAY 2	
1	ATR 1
2	CHECK REG 1
3	T REG (32-63)
4	ROSDR (0-35)
5	X REG (0-31)
6	K REG (0-31)

DISPLAY NO. 3

Roller Pos.	Indicators
1	STORAGE REQUEST: IC, D, FLT, SET KEY, INSERT KEY, 3 CYCLE, PAGE 1 LTH · MANUAL CONTROLS: RPT INSTR ADJ, INIT; PULSE MODE ADJ, INIT; STOP, BLOCK, PASS PULSE, BLOCK INTRPT, FORCE ADDR, INSTR STEP, SINGLE CYCLE, CHK SUMM, INHIB CLOCK · FLT CONTROLS: RPT TEST, FLT TEST, ROS TEST, SCC, SYNC, DEFEAT INTLV NO REV, REV, BACK SPACE, CNSL LOG, SOROS, DIAG, DIAG RELEASE, TIC, GAP
2	Q REGISTER: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31
3	A REGISTER: P 0-7, 0–7, P 8-15, 8–15, P 16-23, 16–23, P 24-31, 24–31
4	HW EXTD: 36, 37 · H LS LAR CONTROL: 38, 39, 40, 41, 42 · L STOR REQ SET MARK: 43, 44, 45, 46 · NA,AD NEXT ROS BASE ADDRESS: 47–56 · K Y BRANCH: 57, 58, 59, 60, 61 · J X OR Z BRANCH: 62–68 · PREV ADR A · FLT MODE
5	PERMIT IOCE: 1, 2, 3 · IOCE MACH CHK: 1, 2, 3 · SEL IOCE: 1, 2, 3 · IOCE: INTRPT REQ, MC REQ · INTRPT GATE TGR · N REGISTER: P 0-7, 0–7, P 8-15, 8–15
6	Y REGISTER: P 32-39, 32–39, P 40-47, 40–47, P 48-55, 48–55, P 56-63, 56–63

DISPLAY 3	
1	STOR REQ, MAN CTLS, FLT CTLS
2	Q REG (0-31)
3	A REG (0-31)
4	ROSDR (36-68)
5	IOCE CTLS, N REG (0-15)
6	Y REG (32-63)

Diagram 6-2. CE Roller Switch Indicators (Sheet 1 of 2)

A — DISPLAY NO. 4

1	PROGRAM STATUS WORD																																											1
	SYSTEM MASK								EXT	P					ASCII	MC	WAIT	PROB	NO	IC IN	COND 2	CODE 1	PSW PROGRAM MASK FXP OVFLW	DEC OVFLW	EXP UNFLW	LOST SIG	MACH CHK INTRPT	SUPV CALL INTRPT			PROGRAM INTRPT				INTRPT PRI			
	P 0-7	0	1	2	3	4	5	6	7	8-15	8	9	10	11	12	13	14	15	RETRY	LSWR	34	35	36	37	38	39					8	4	2	1	1	2		
2	Q REGISTER																																											2
	P 32-39	32	33	34	35	36	37	38	39	P 40-47	40	41	42	43	44	45	46	47	P 48-55	48	49	50	51	52	53	54	55	P 56-63	56	57	58	59	60	61	62	63		
3	B REGISTER																																											3
	P 32-39	32	33	34	35	36	37	38	39	P 40-47	40	41	42	43	44	45	46	47	P 48-55	48	49	50	51	52	53	54	55	P 56-63	56	57	58	59	60	61	62	63		
4	M A SIDE CTL SERIAL ADDER					N B SIDE CTL SERIAL ADDER				P PADDL CONTROL			EW EXTD	Q GATE ONES PA				R AB→F	T AB, IC, F→PB					U ST, DA→PA				V E, Q→PB				EDIT								4
	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	43-68	86	87	88	89	90	69-99	92	93	94	95	96	97	98	99		RT DIG	S	LEAVE	STEP ABC		
5	STATUS TRIGGERS								INSTRUCTION FETCH CONTROLS										EXTERNAL INTERRUPTS														PIR						5
	A	B	C	D	E	F	G	H	BLOCK	1	2	3	EXEC		PS CMPR	IN STOR FETCH	BR INVLD ADDR	INVLD ADDR	IL NOT AVAIL	CE 1 WD	CE 1 RD	CE 2 WD	CE 2 RD	TC AT LIMIT	CONS SIG	CE 3 WD	CE 3 RD	CE 4 WD	CE 4 RD	PIR	DAR	IOCE 1	IOCE 2	IOCE 3		TIME GATE TGR		
6	EXTERNAL REGISTER																																											6
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15	P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31		

	DISPLAY 4
1	PSW
2	Q REG (32-63)
3	B REG (32-63)
4	ROSDR (69-99), EDIT
5	STATUS, INSN FETCH, EXTERNAL INTERRUPTS
6	EXTERNAL REG 0-31

B — DISPLAY NO. 5

1	PHYSICAL PSBAR					PSBAR COUNTER					LOGICAL PSBAR																								SYSTEM MASK				PROGRAM INTRPT				1
	P 9-12	9	10	11	12	P 9-12	9	10	11	12	P 9-15	9	10	11	12	13	14	15	P 16-19	16	17	18	19	ALT PSBA					16	17	18	19	SE STOP	PSA LOCKOUT 1	2	3		
2	REV SABTP	LCMPR	REV SAFSP	REV MRKP	REV SARPA	REV SARPB	LOG CNT		DSBL TMR	ADDR SEQUENCE				FLT COUNTER				FLT CHK			ROS TEST SEQ												FLT STG ERR						2
	CE TEST ADDR				LFTHF	UNCT	CONDT	ERSLT		0	1	2	3	4	0	1	2	3	0	1		0	1	2						PASS	FAIL				MMSC	BFR 1		
3	R REGISTER																		E REGISTER																									3
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15		
4	S 0-31	T32-63		T32-63		T32-47	T48-63	K00-31	D8-31		D8-31		D8-31		FMTO	FMTN	FMTW	IC	A0-31	A4-7	A8-31	B32-63	B64-67	A6-31	B32-67	B64-67	EXCS-6	F4-7	HOT 1	E8-11	E12-15	F8-11	Q4-15	Q20-31	Q36-47	Q52-63		
	32-63	32-63		31-62		48-63	48-63	32-63	8-31		7-30		40-63		PA		PB	40-63	32-63	4-7	8-31	32-63	64-67	4-29	30-65	28-31	28-63	60-63	60	56-59	60-63		52-63		52-63			
		C	TL1	CL1					T	C	TL1	CL1	T	C										L2	L2													
5	CONFIGURATION CONTROL REGISTER																																											5
	P 0-7	STATE 0	1	SCON 1	2	3	4	ILOS		P 8-15	1	2	SE 3	4	5	6	7	SE/DE 8	P 16-23	9	10			CE 1	2	3	4	P 24-31						IOCE 1	2	3		
6	DIAGNOSE ACCESSIBLE REGISTER MASK																																											6
	P 0-7	IOCE 1		IOCE 2		IOCE 3		1	2	P 8-15	3	4	SE 5	6	7	SE/DE 8	9	10	P 16-23			1	PAM/RCU 2	3	1	TCU 2	3	P 24-31	CE OWN OTC	OBS		1	2	CE 3	4		

	DISPLAY 5
1	PSBAR, SYS MASK, INTRPTS
2	MCW AND FLT CONTROL
3	R REG, E REG
4	GATE CONTROL TGRS
5	CCR
6	DAR MASK

D — DISPLAY NO. 6

1	PARALLEL ADDER LATCHES																																											1
	P 32-39	32	33	34	35	36	37	38	39	P 40-47	40	41	42	43	44	45	46	47	P 48-55	48	49	50	51	52	53	54	55	P 56-63	56	57	58	59	60	61	62	63		
2	MARKS									ST PTY	LS ADDRESS REGISTER					LS	INHIB STORE	TX	B REG						ABC			PADDL					LS	STC				
	P 0-7	0	1	2	3	4	5	6	7	32-39	0	1	2	3	4	WRITE	WRITE	TGR	P 64-67	64	65	66	67		0	1	2	P 64-67	64	65	66	67	SIGN	0	1	2		
3	SERIAL ADDER LATCHES									INSTRUCTION COUNTER																																		3
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15	P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31		
4	DIAGNOSE ACCESSIBLE REGISTER																																											4
	P 0-7	IOCE 1 a	b	IOCE 2 a	b	IOCE 3 a	b	1	2	P 8-15	3	4	SE/DE ELC 5	6	7	8	9	10	P 16-23			1	PAM/RCU ELC 2	3	1	TCU ELC 2	3	P 24-31	CE OWN OTC	OBS		1	2	CE ELC 3	4		
5	CHECK REGISTER 2																																											5
		STOR UNIT CHECK ID 0	1	2	3	360 MODE	TEST MODE	SE STOP 360			SAB PTY CHK	SDBI PTY CHK	STG T O	STG ADDR CHK	STG DATA CHK	FETCH CHK	LOS SENT			IOCE CHK RESP	LS BUS CHK	CCR PTY CHK	ATR PTY CHK	PSBAR PTY CHK	PSBAR NOT CONF	PSA ALT	SPLIT LOGOUT		LOG ROS CHK	LOG ADDR CHK	CE LOG REQ	RDD T O						
6	MAINTENANCE CONTROL WORD																																											6
	P 32-39	LOGOUT OR WRAP SELECTED STG ID 0	1	2	3	0	DG SELECTED 1	2	3	DE WRAP P 40-47	1	2	CVG SELECTED 3	4	5	6	REV NORM OP	FORCE DG REQ	P 48-55	DIAG SE 1	INV EXT PTY	RST CHKS	WRAP DE																	

	DISPLAY 6
1	PADDL (32-63)
2	MARK, LAR, B REG, ABC, PADDL, STC
3	SADDL, IC
4	DAR
5	CHECK REG 2
6	MCW (32-51)

Diagram 6-2. CE Roller Switch Indicators (Sheet 2 of 2)

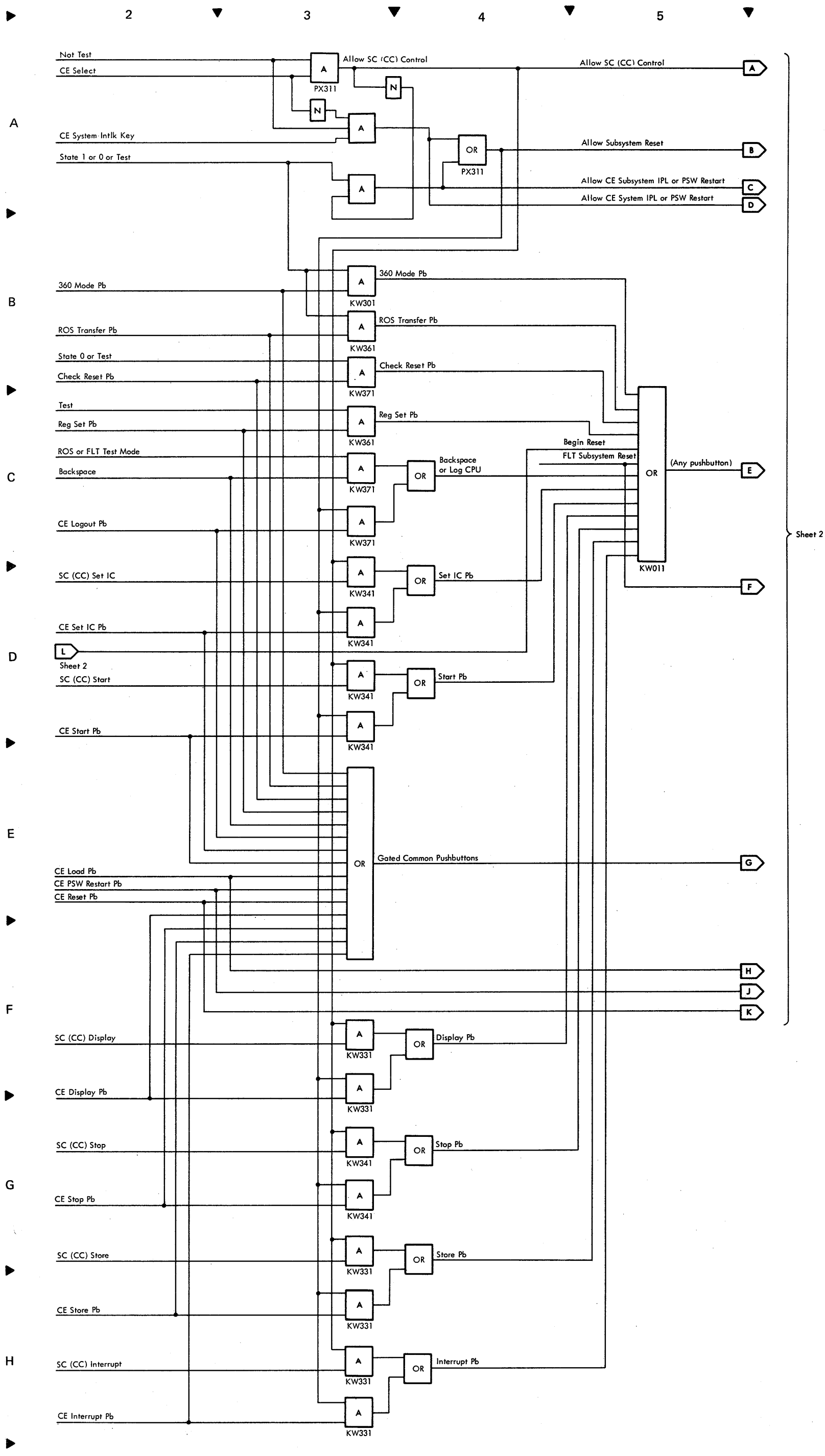


Diagram 6-3. Pushbutton Signal Generation (Sheet 1 of 2)

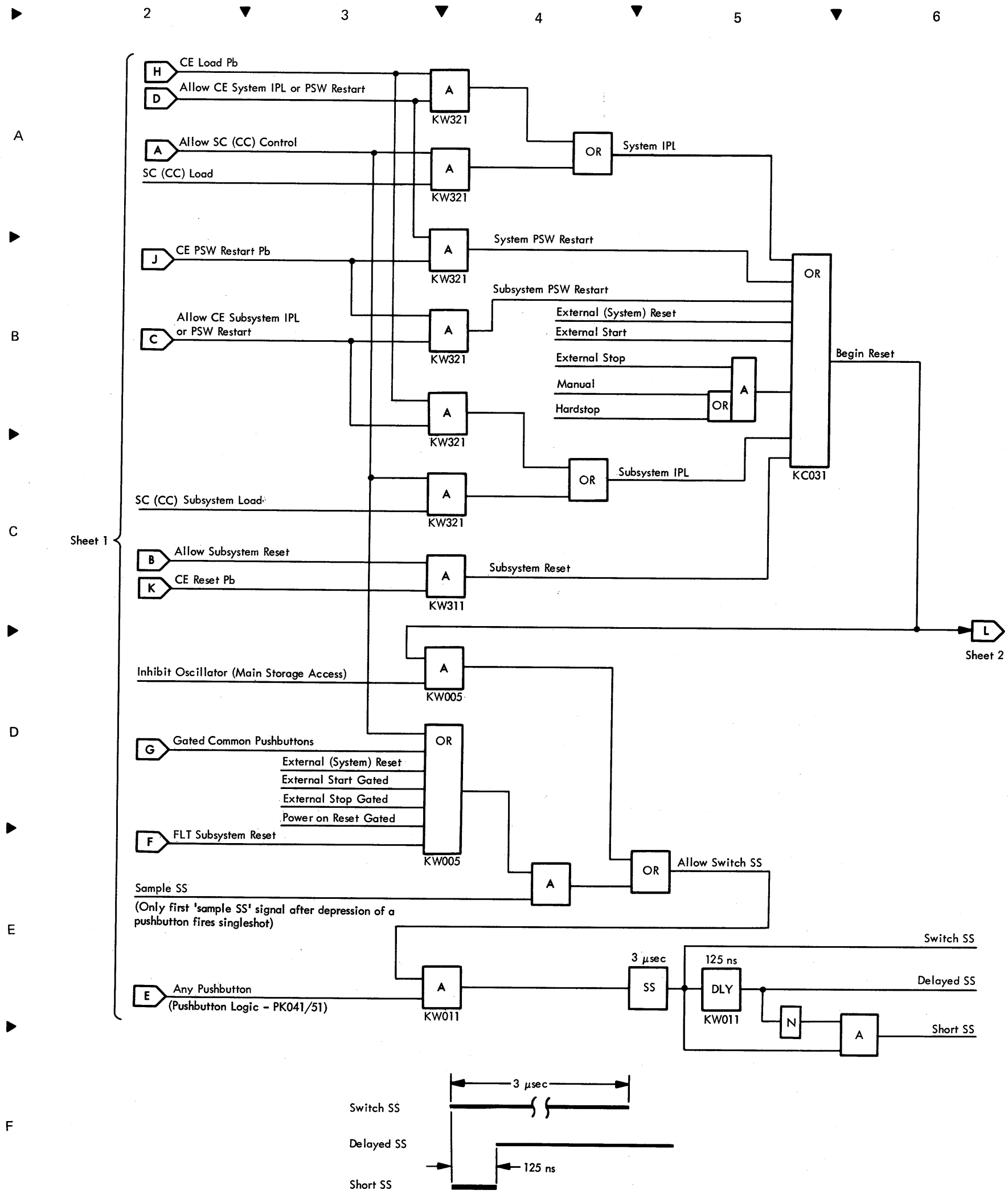


Diagram 6-3. Pushbutton Signal Generation (Sheet 2 of 2)

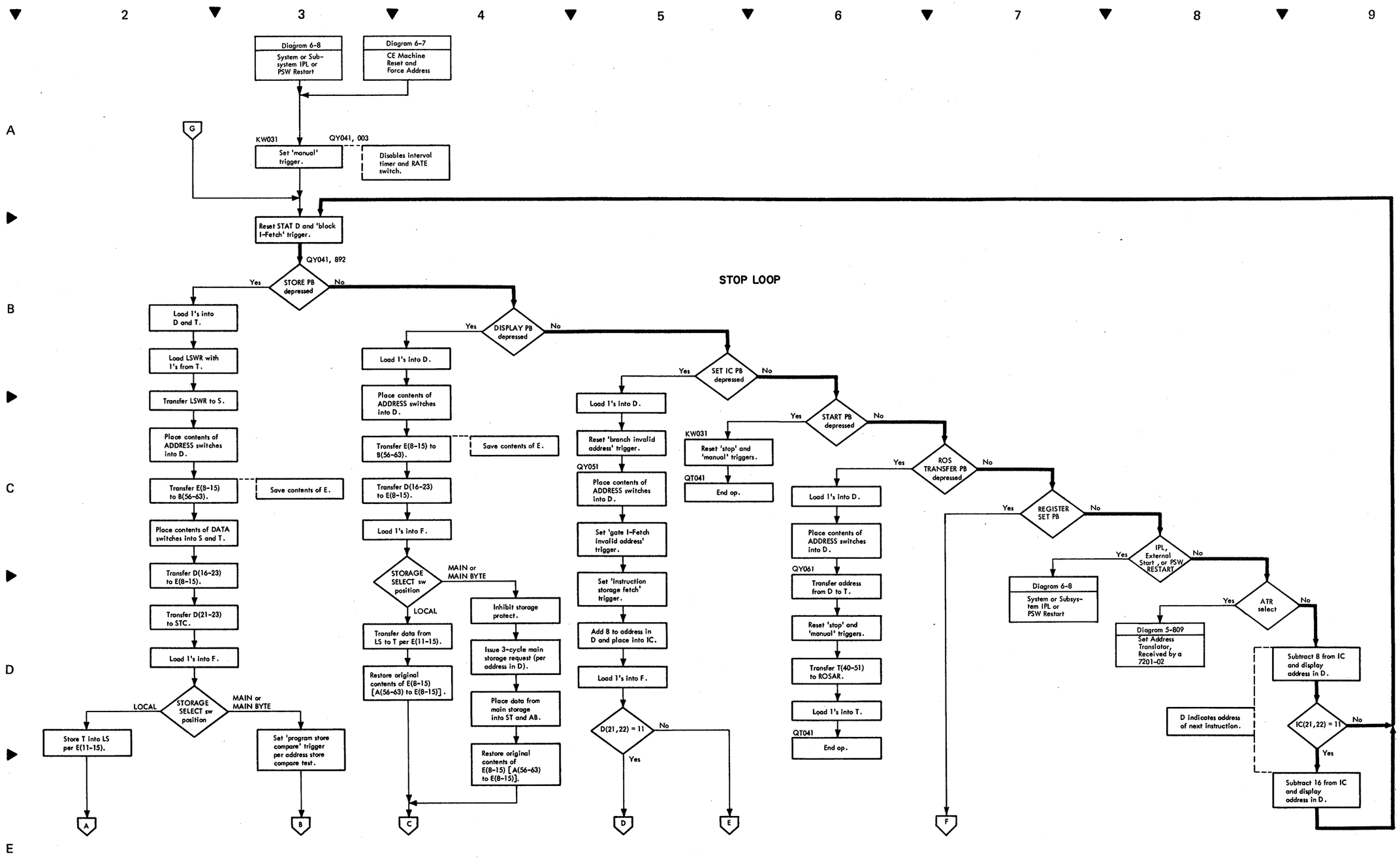


Diagram 6-4. Stop Loop Routine (Sheet 1 of 2)

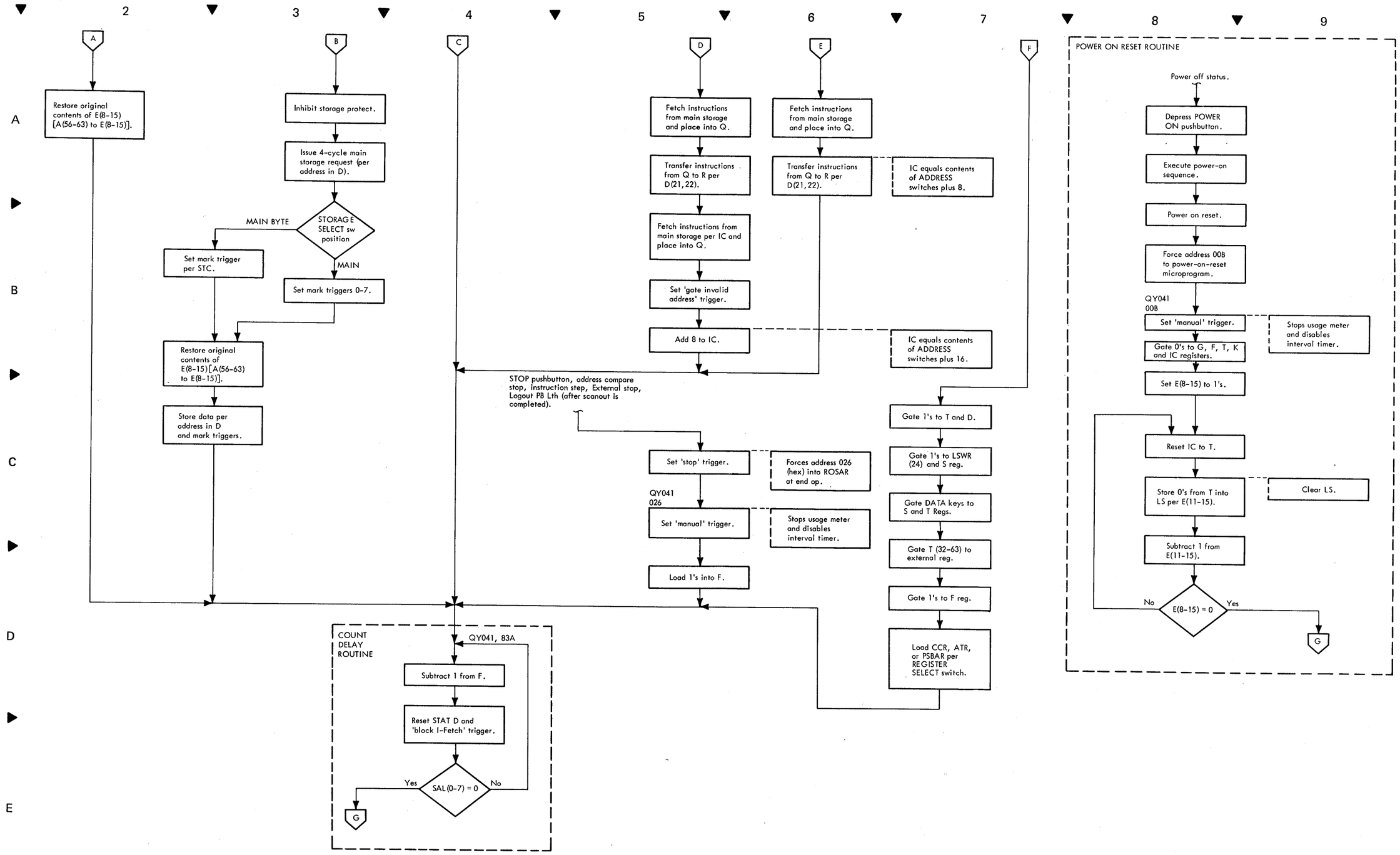


Diagram 6-4. Stop Loop Routine (Sheet 2 of 2)

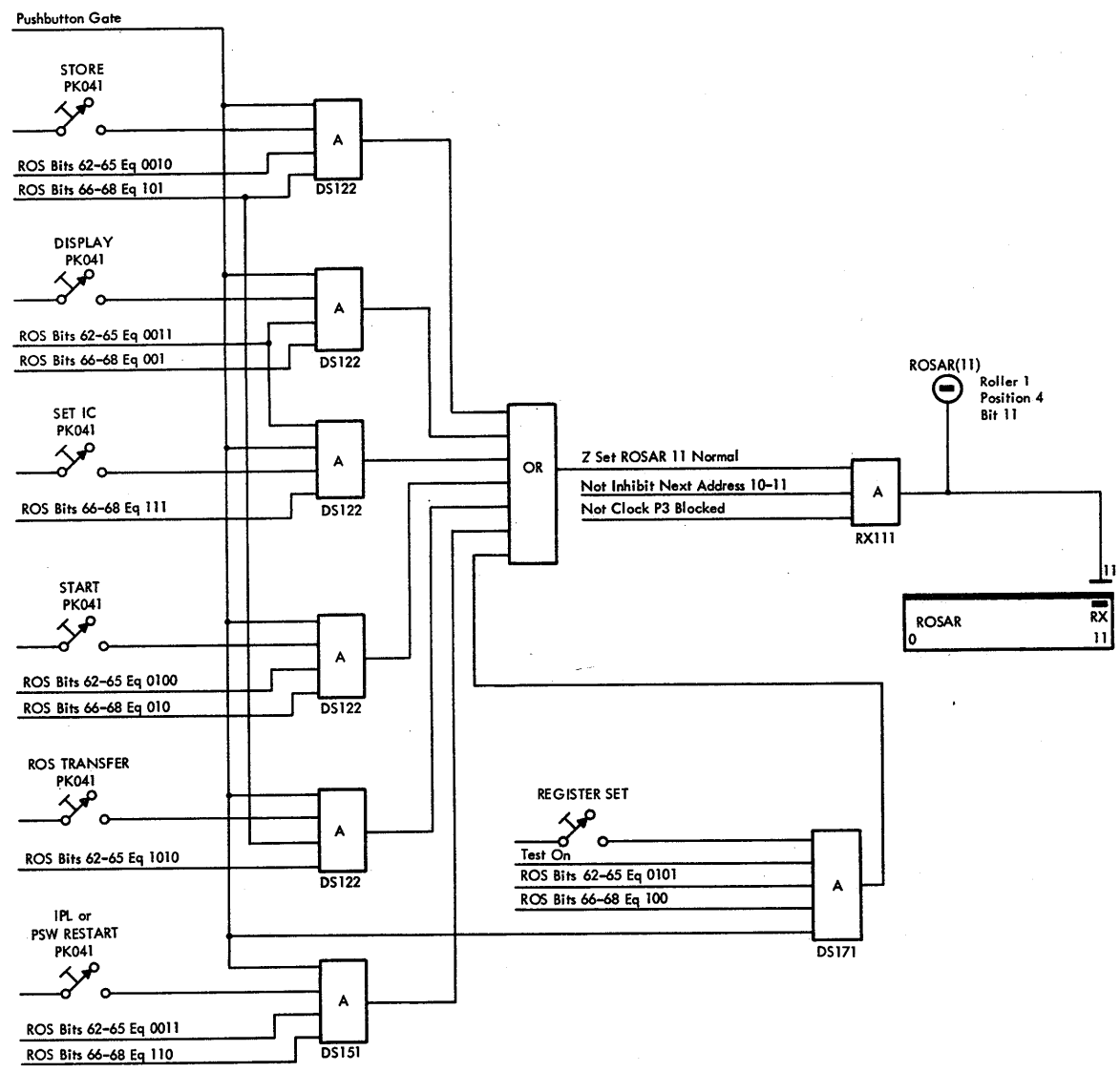


Diagram 6-5. Stop Loop Monitored Pushbutton Gating

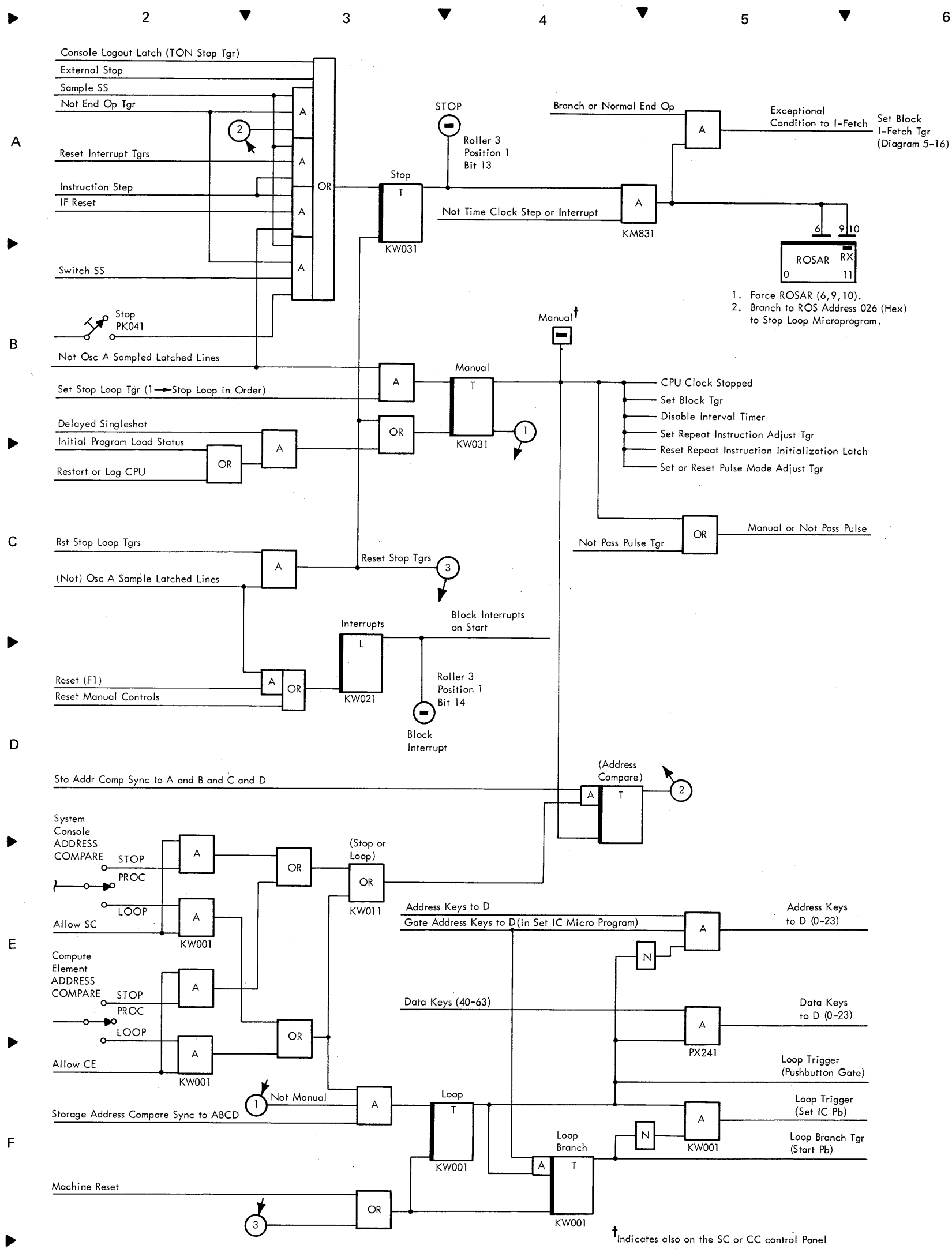


Diagram 6-6. Stop, Manual, Address Compare Triggers, and Block Interrupt Latch (Sheet 1 of 2)

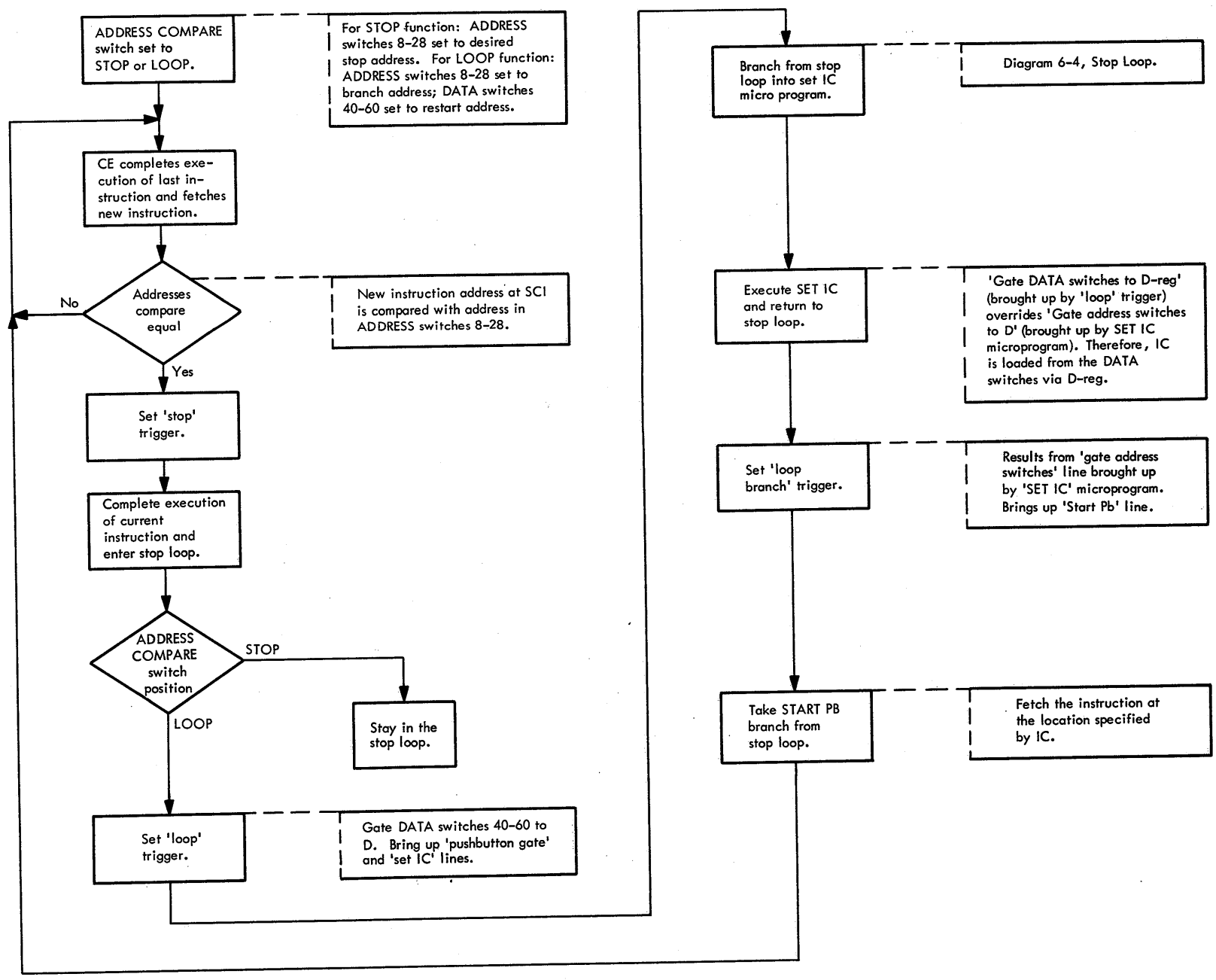
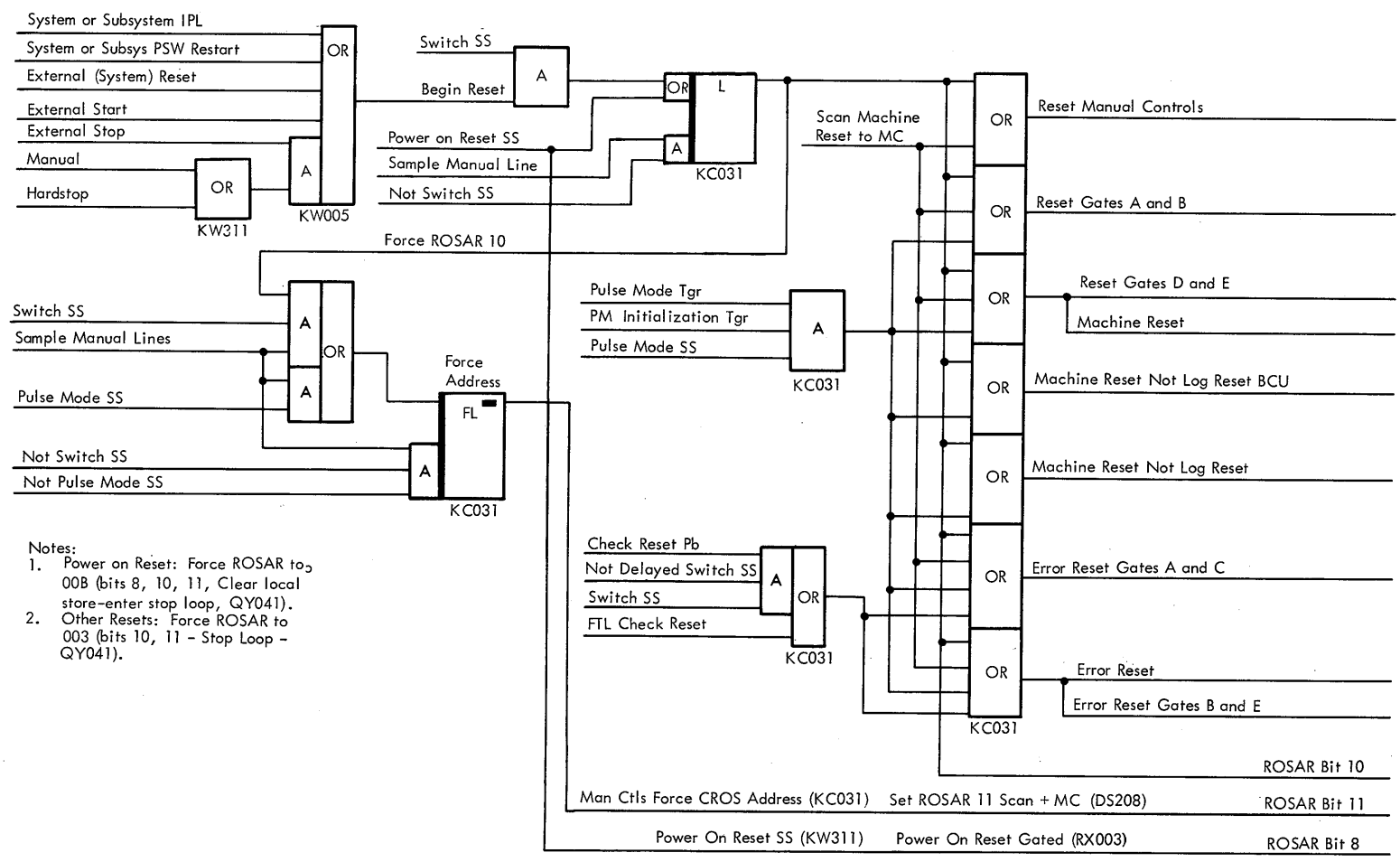
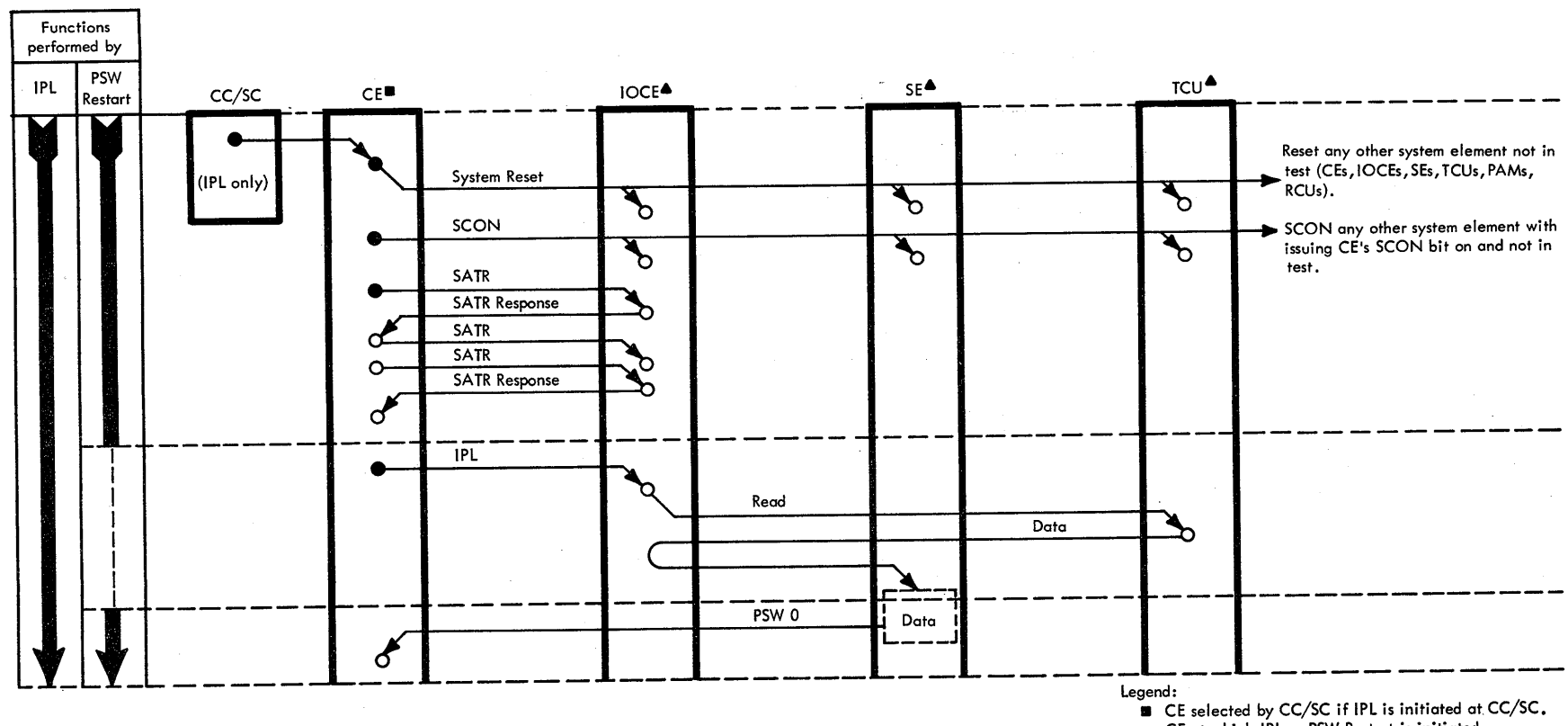


Diagram 6-6. Stop, Manual, Address Compare Triggers, and Block Interrupt Latch (Sheet 2 of 2)



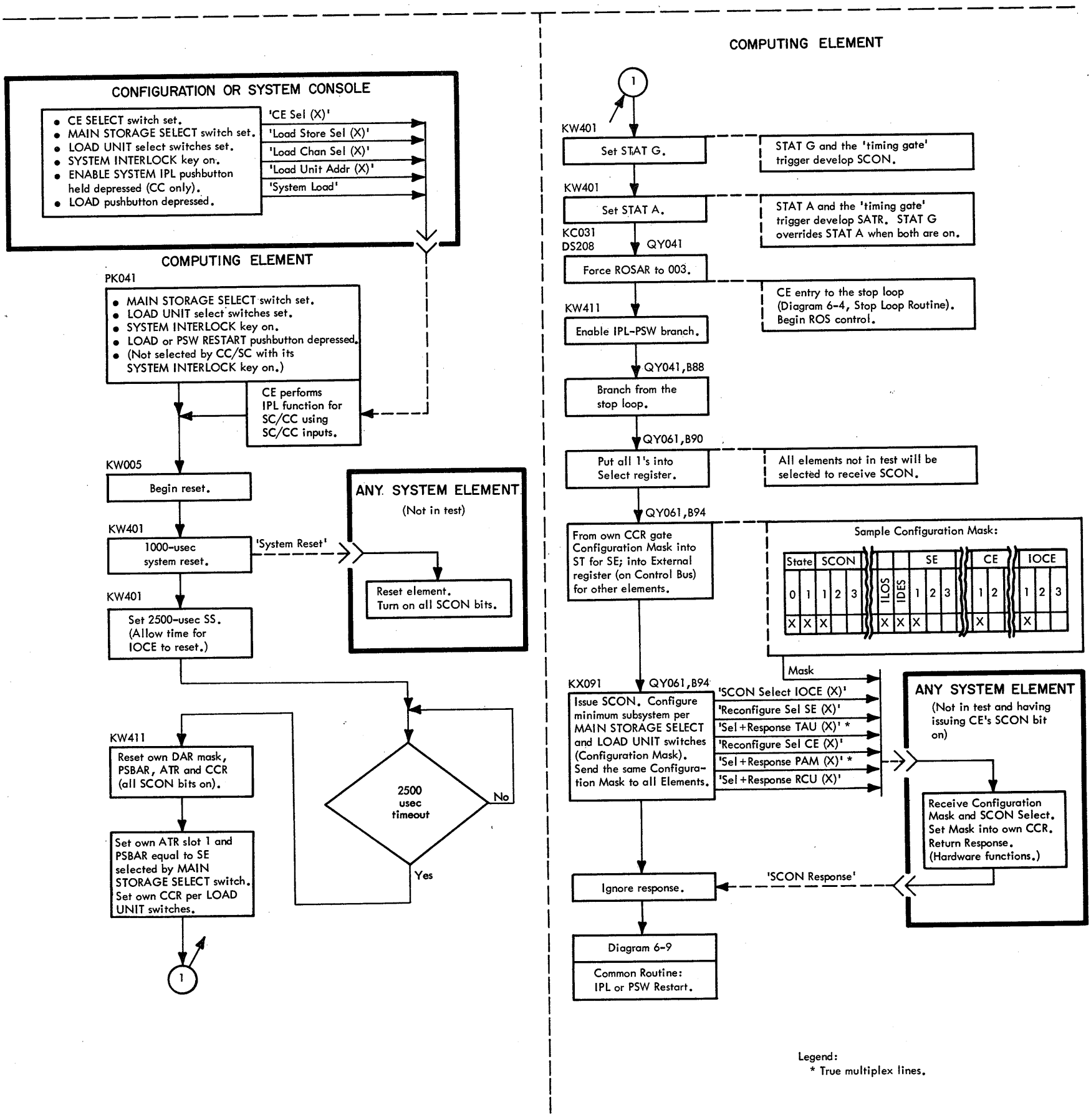
Notes:
1. Power on Reset: Force ROSAR to 00B (bits 8, 10, 11, Clear local store-enter stop loop, QY041).
2. Other Resets: Force ROSAR to 003 (bits 10, 11 - Stop Loop - QY041).

Diagram 6-7. CE Machine Reset and Force Address



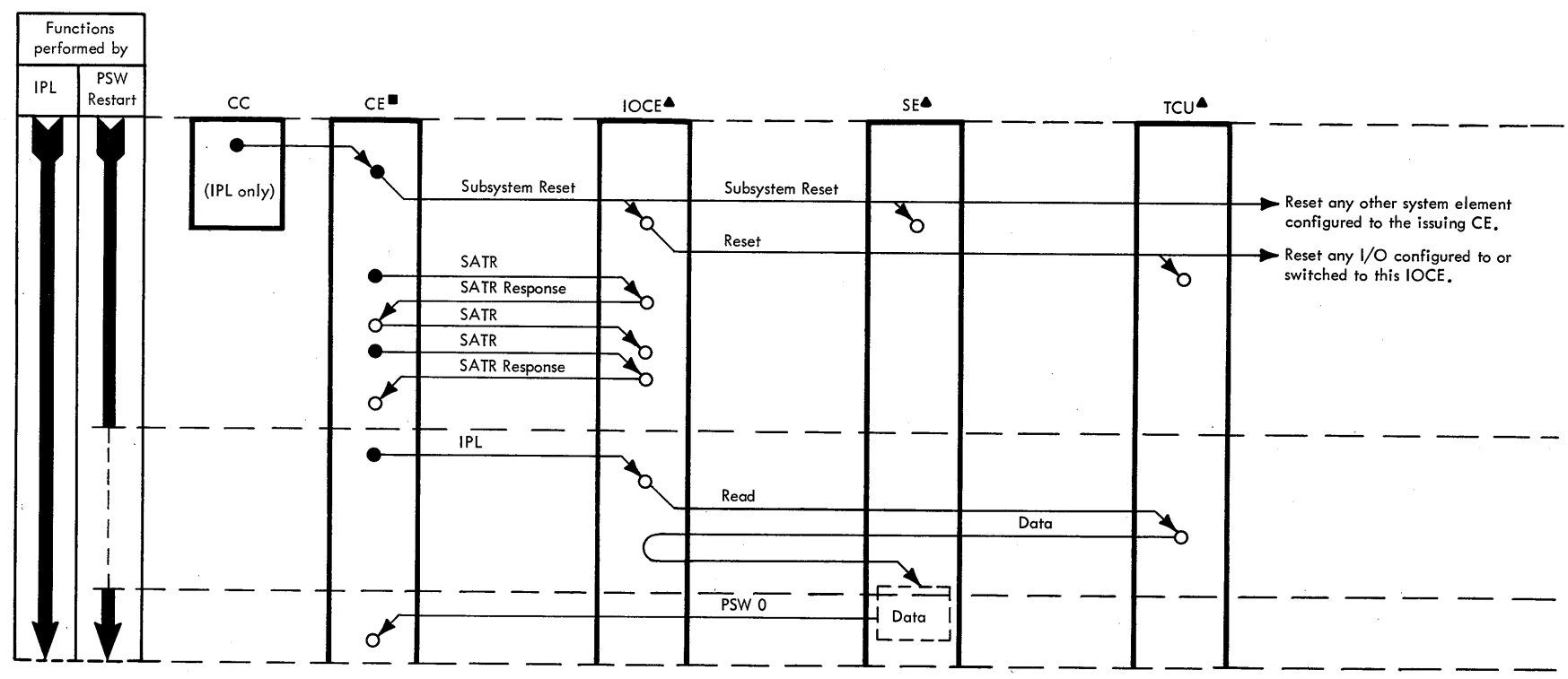
Summary of System Operations: IPL or PSW Restart

Legend:
■ CE selected by CC/SC if IPL is initiated at CC/SC. CE at which IPL or PSW Restart is initiated.
▲ IOCE and TCU selected by SC/CC or CE LOAD UNIT switches. SE selected by SC/CC or CE MAIN STORAGE SELECT switch.
● Signal origin
○ Signal destination



Legend:
* True multiplex lines.

Diagram 6-8A. System Operation: IPL or PSW Restart



Summary of Subsystem Operations: IPL or PSW Restart.

Legend:
- ■ CE which is selected by CC if IPL is initiated at the CC.
  CE at which IPL or PSW Restart is initiated.
- ▲ IOCE and TCU selected by CC or CE LOAD UNIT switches and SE selected by CC or CE MAIN STORAGE SELECT switch.
- ● Signal origin
- ○ Signal destination

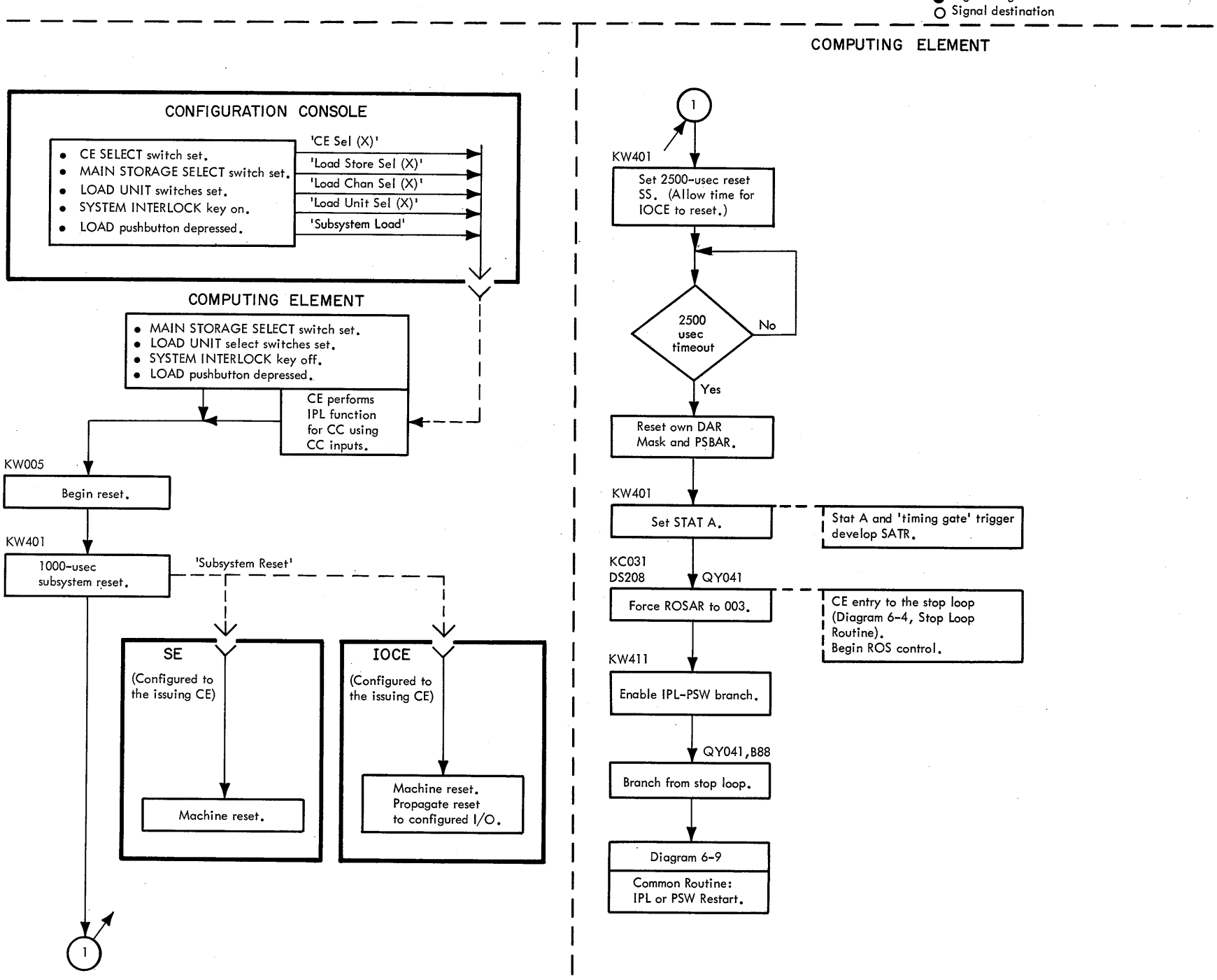


Diagram 6-8B. Subsystem Operation: IPL or PSW Restart

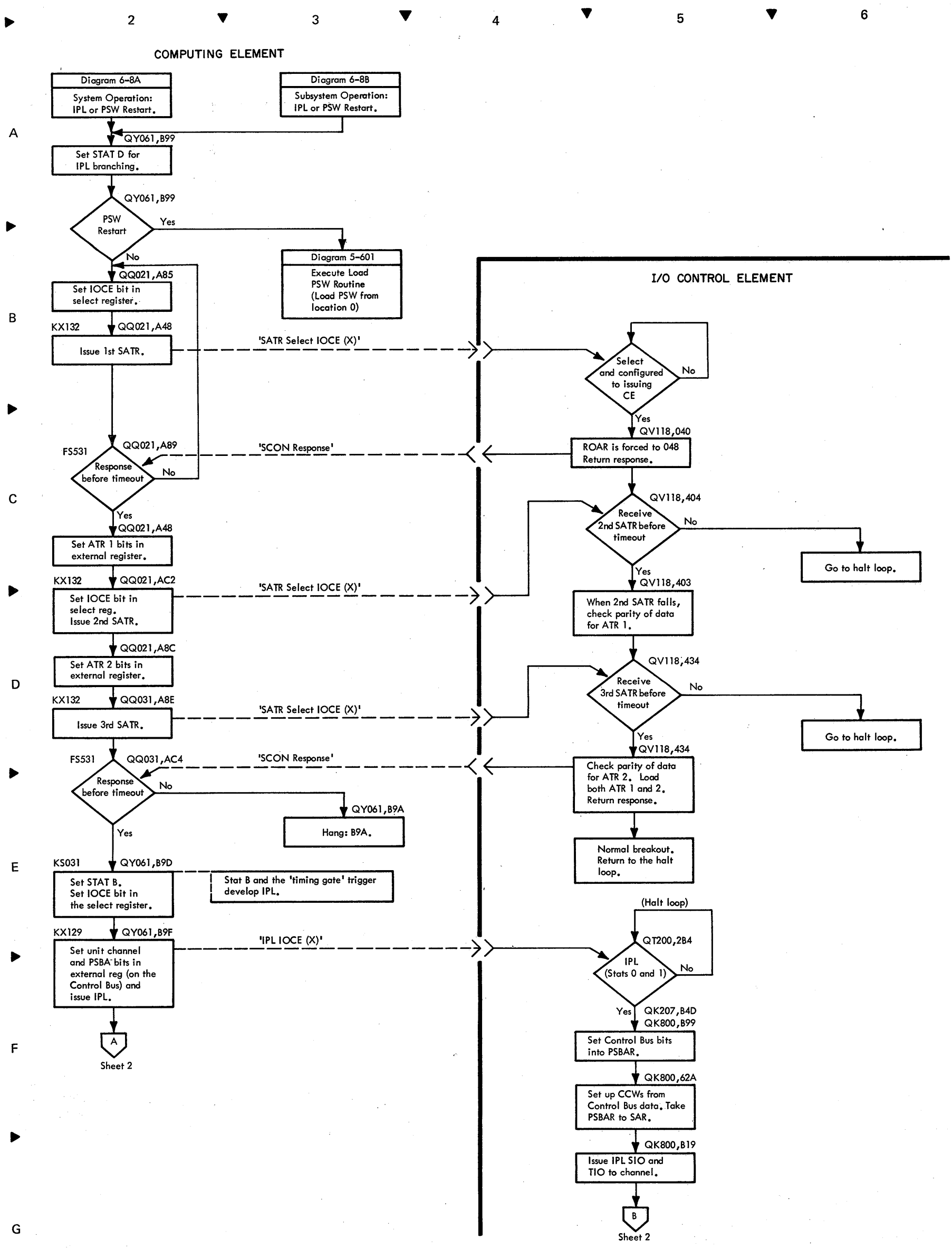
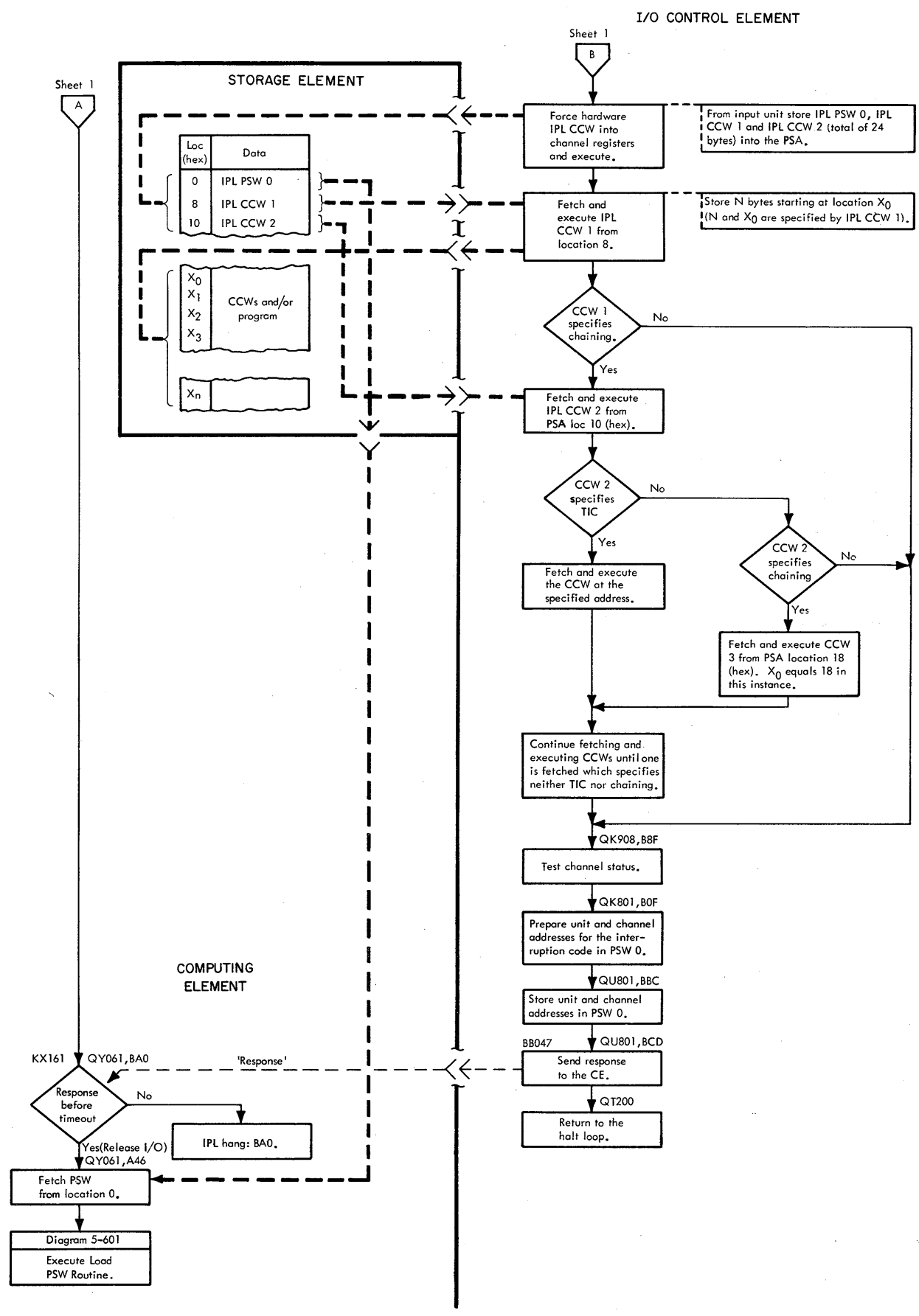


Diagram 6-9. Common Routine: IPL or PSW Restart (Sheet 1 of 2)

H



Legend: Heavy dashed lines indicate data flow.

Diagram 6-9. Common Routine: IPL or PSW Restart (Sheet 2 of 2)

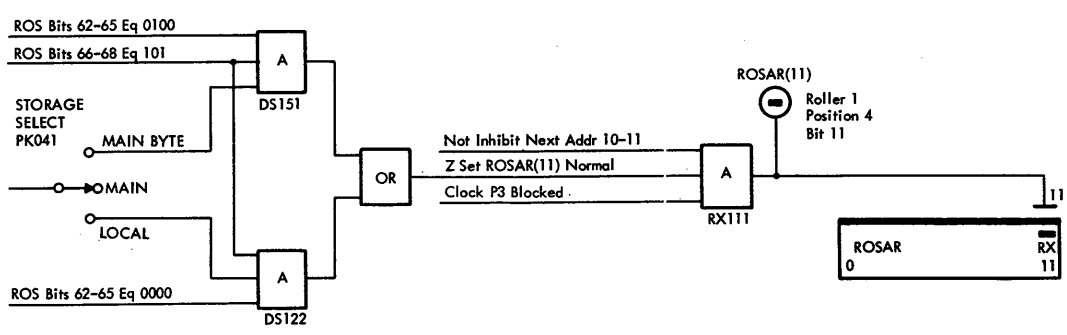


Diagram 6-10. STORAGE SELECT Switch Gating

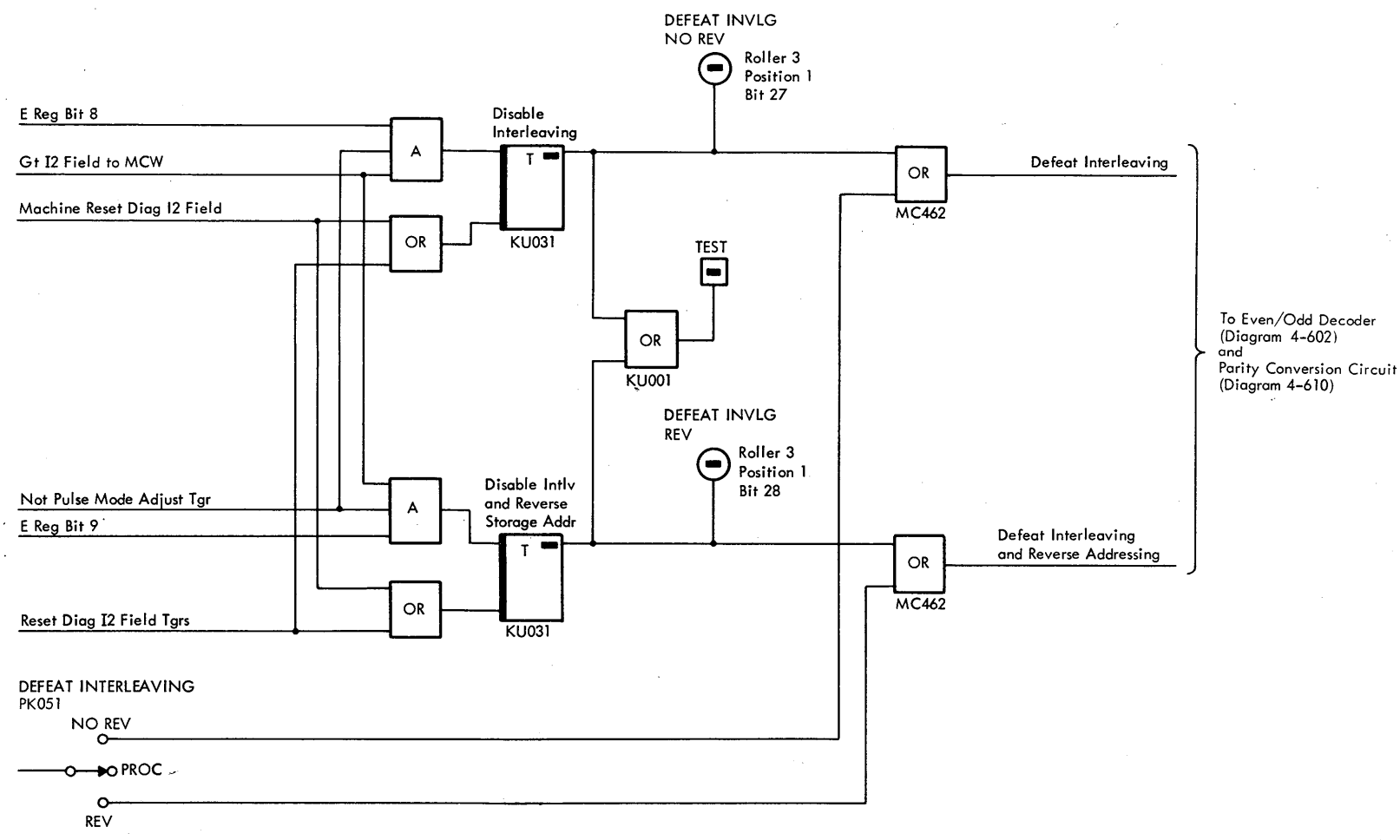


Diagram 6-11 DEFEAT INTERLEAVING Switch Gating

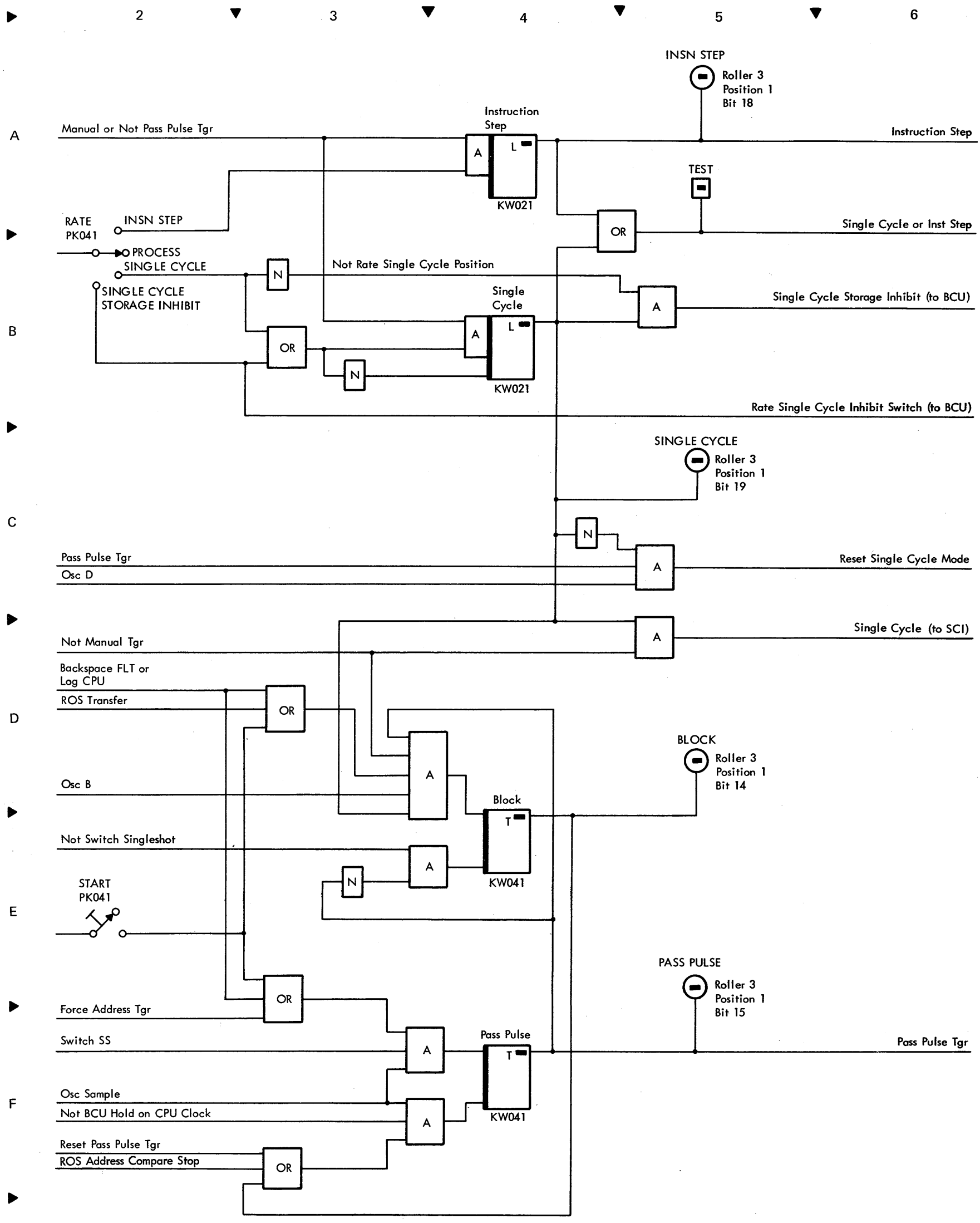


Diagram 6-12. RATE Switch Logic

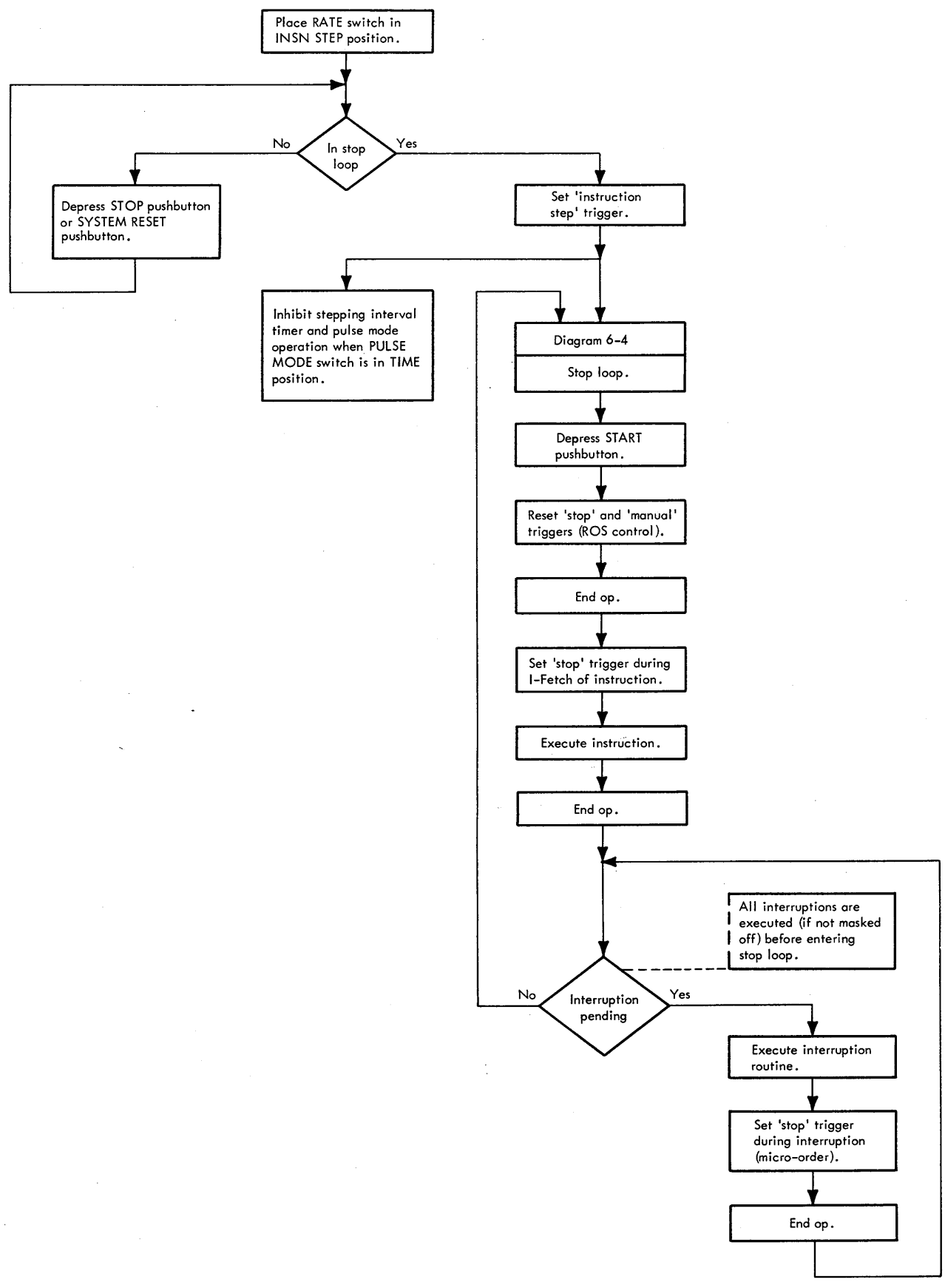


Diagram 6-13. Instruction Step Routine

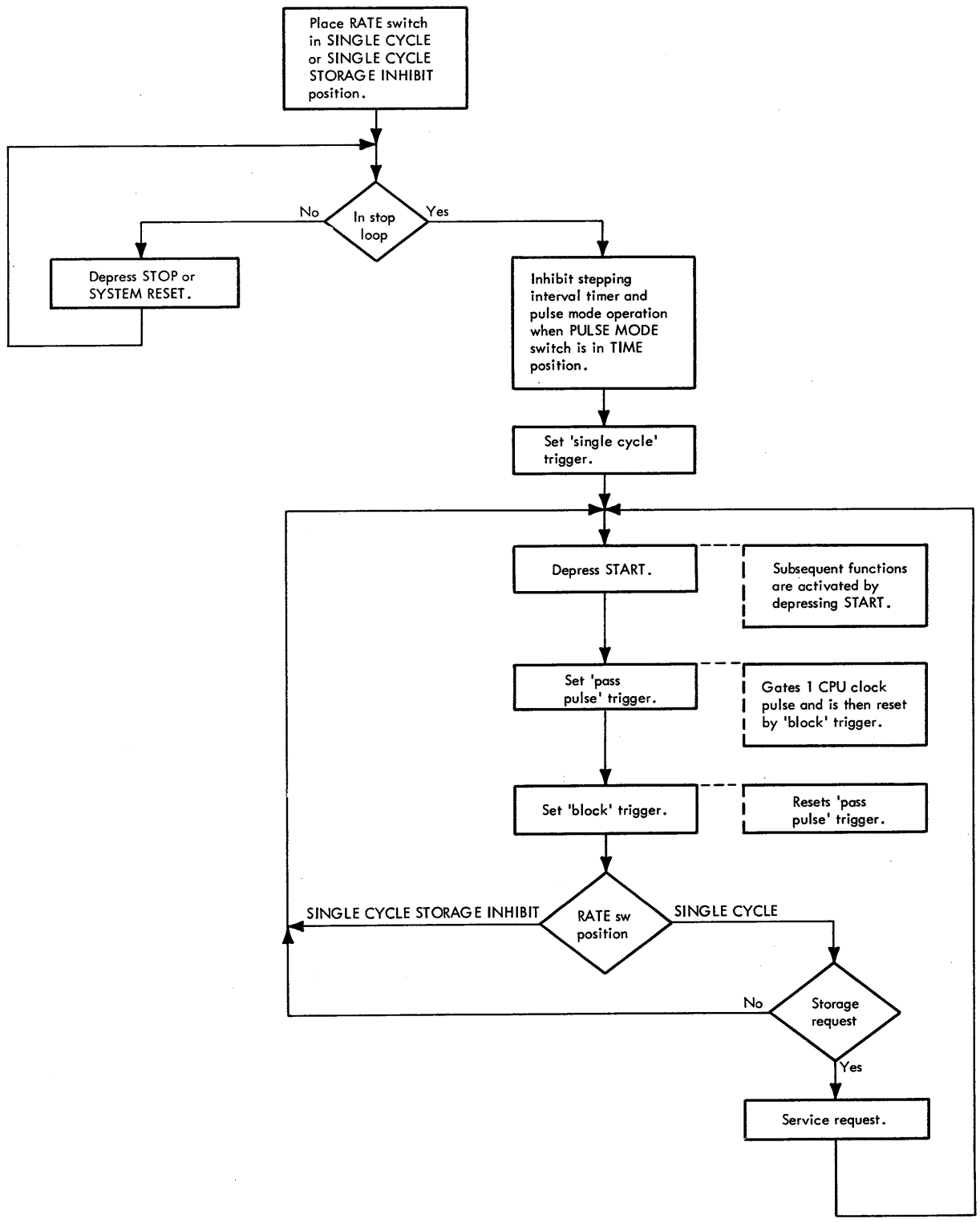


Diagram 6-14. Single-Cycle and Single-Cycle-Inhibit Routine

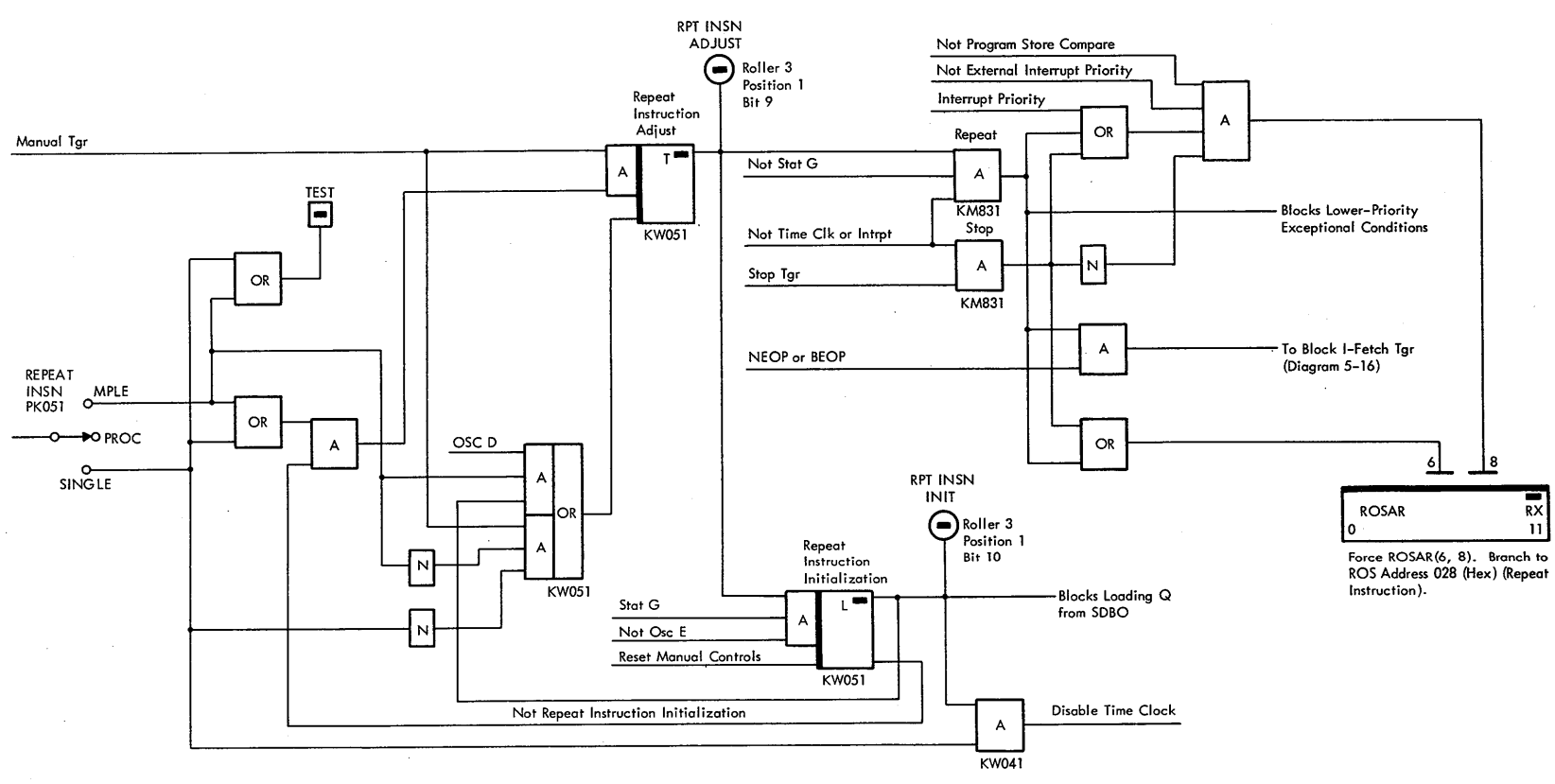


Diagram 6-15. Repeat Instruction Switch Logic

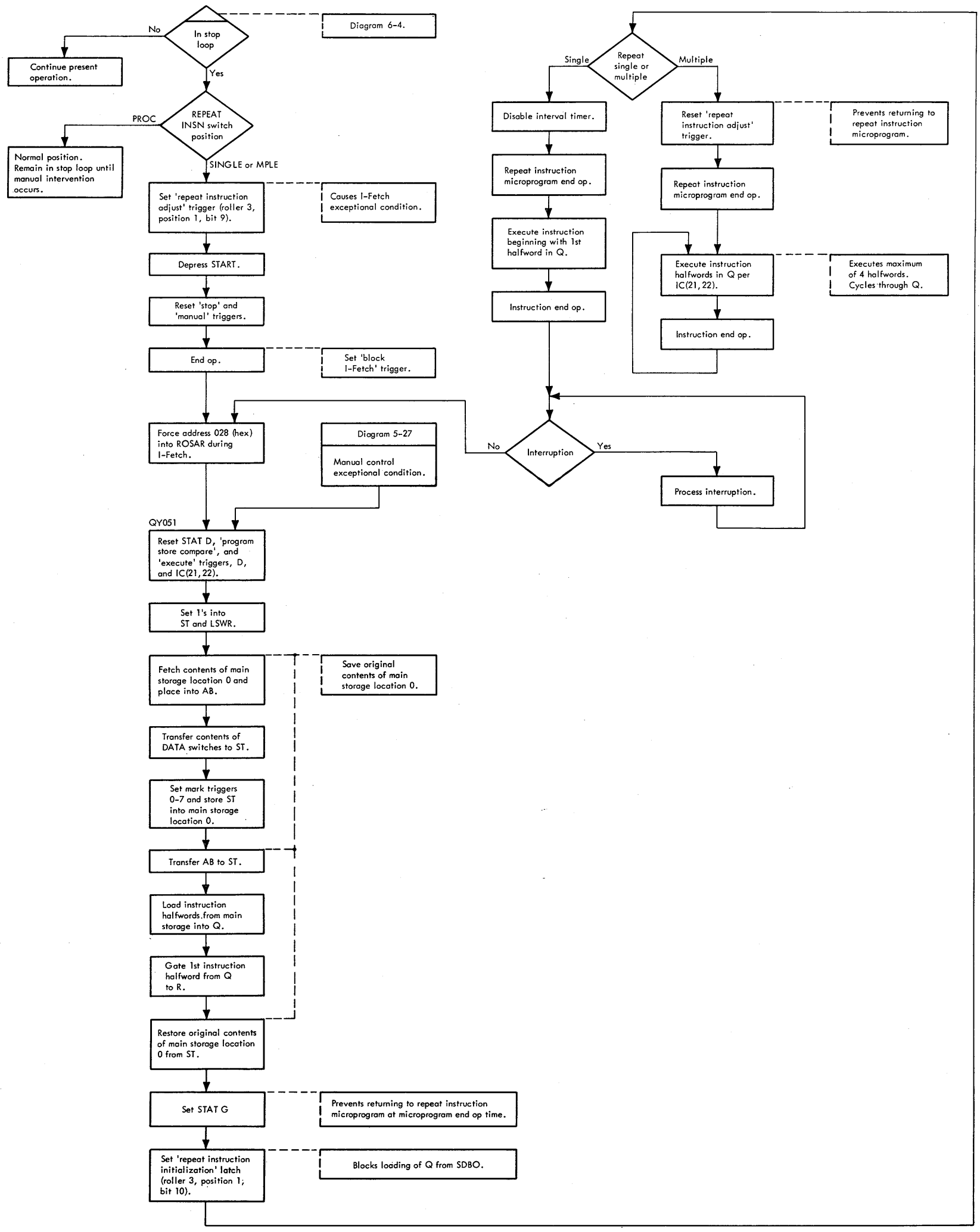


Diagram 6-16. Repeat Instruction Switch Routine

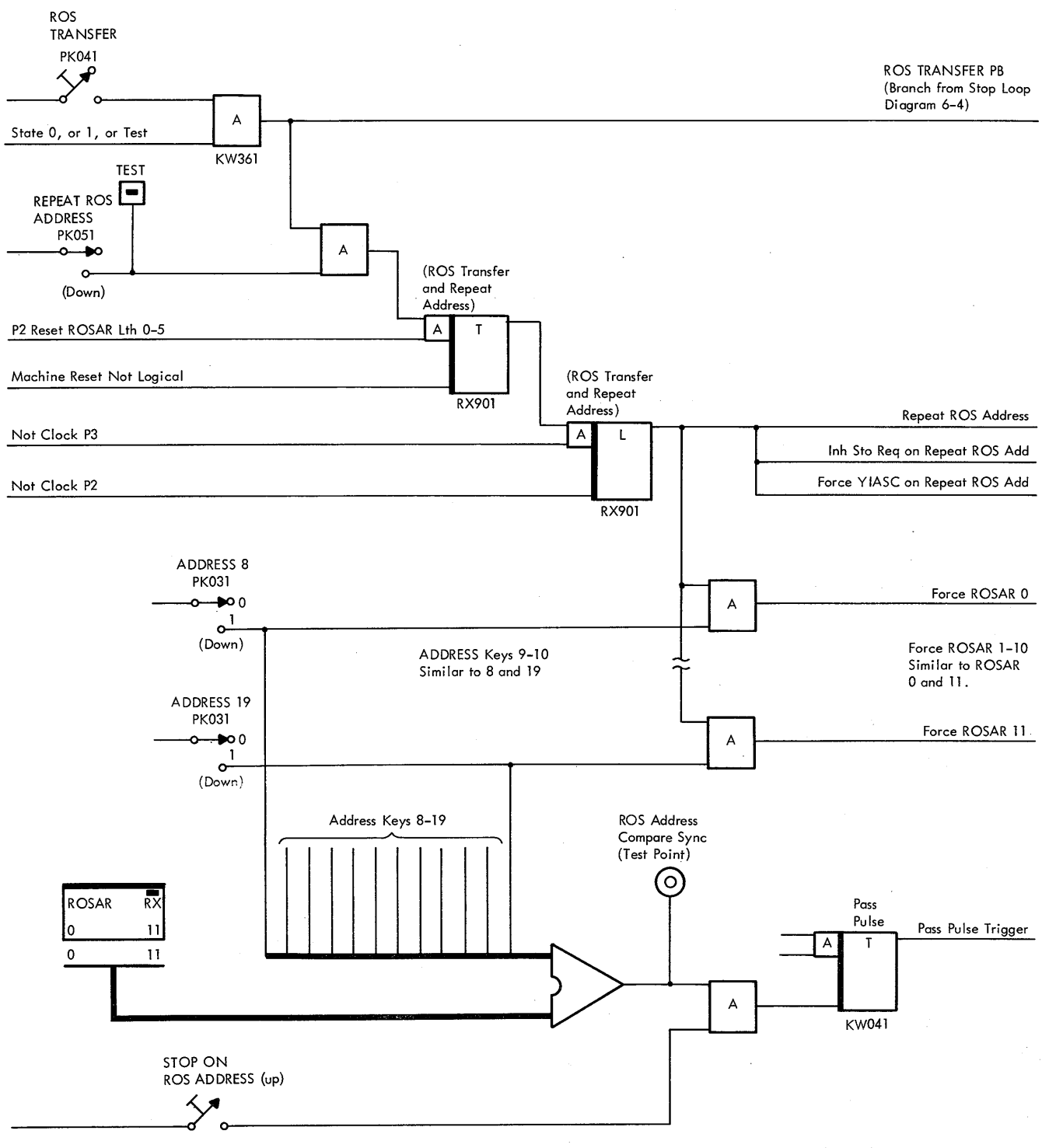
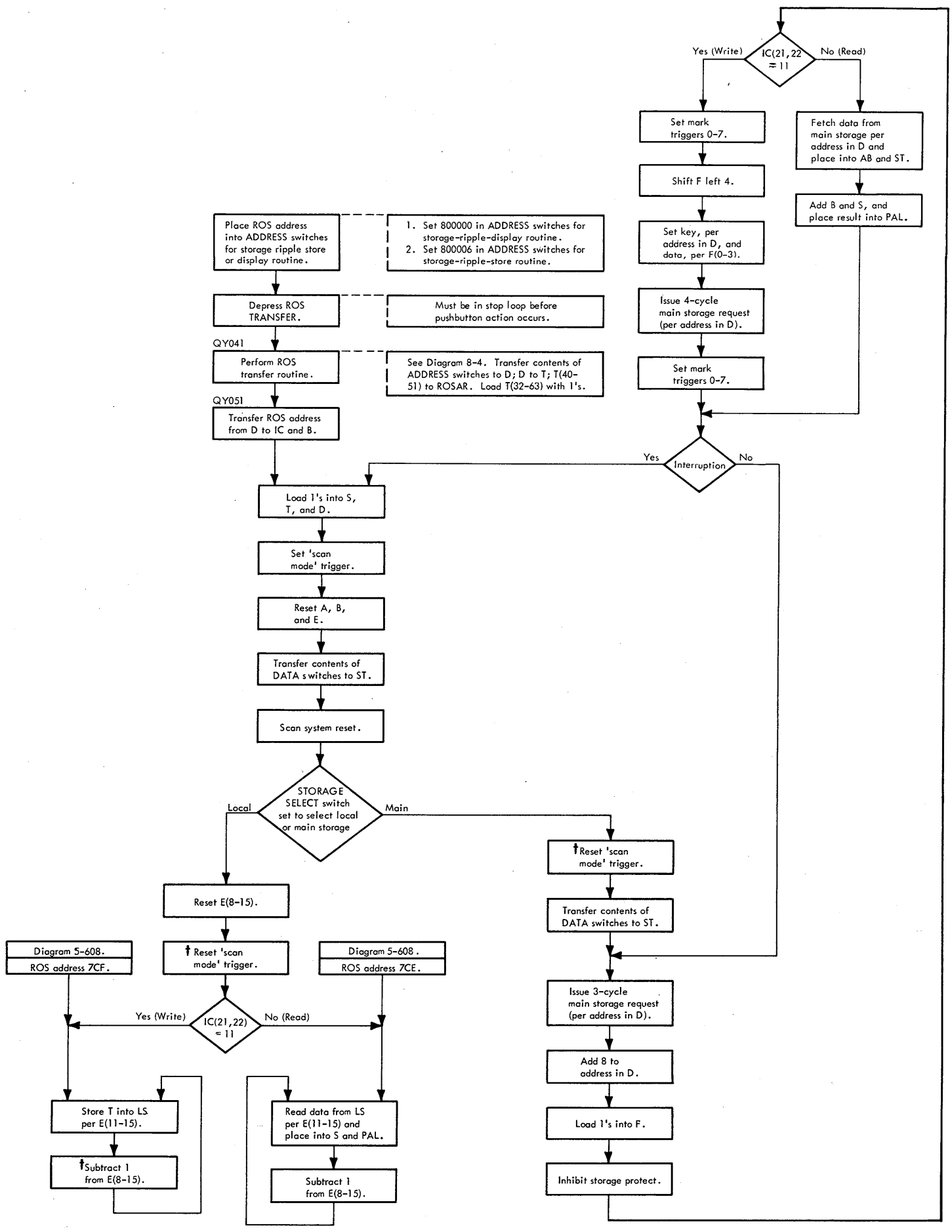


Diagram 6-17. ROS TRANSFER and REPEAT ROS ADDRESS Switch Gating



Note: Manual intervention (e.g., system reset or load) is required to get out of storage ripple loop.

† Following this block, an FLT-2, -3, or -4 microprogram is executed. These microprograms are inserted at this point to exercise circuits; they do not affect the storage ripple test.

Diagram 6-18. Storage Ripple Loop (Store and Display) Routine

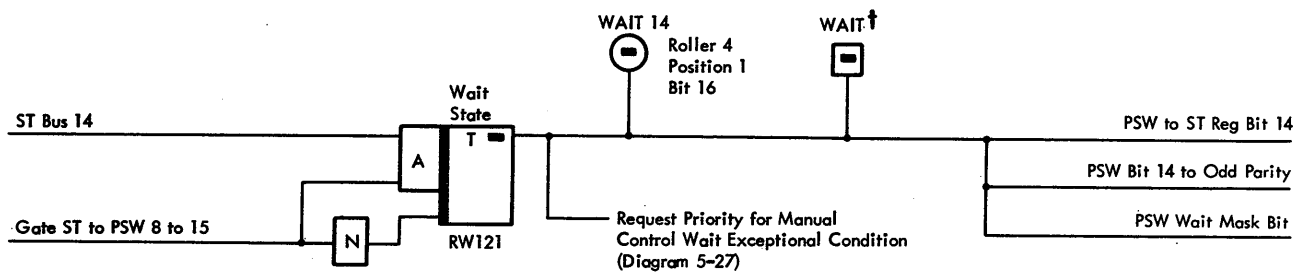


Diagram 6-19. Wait State Gating

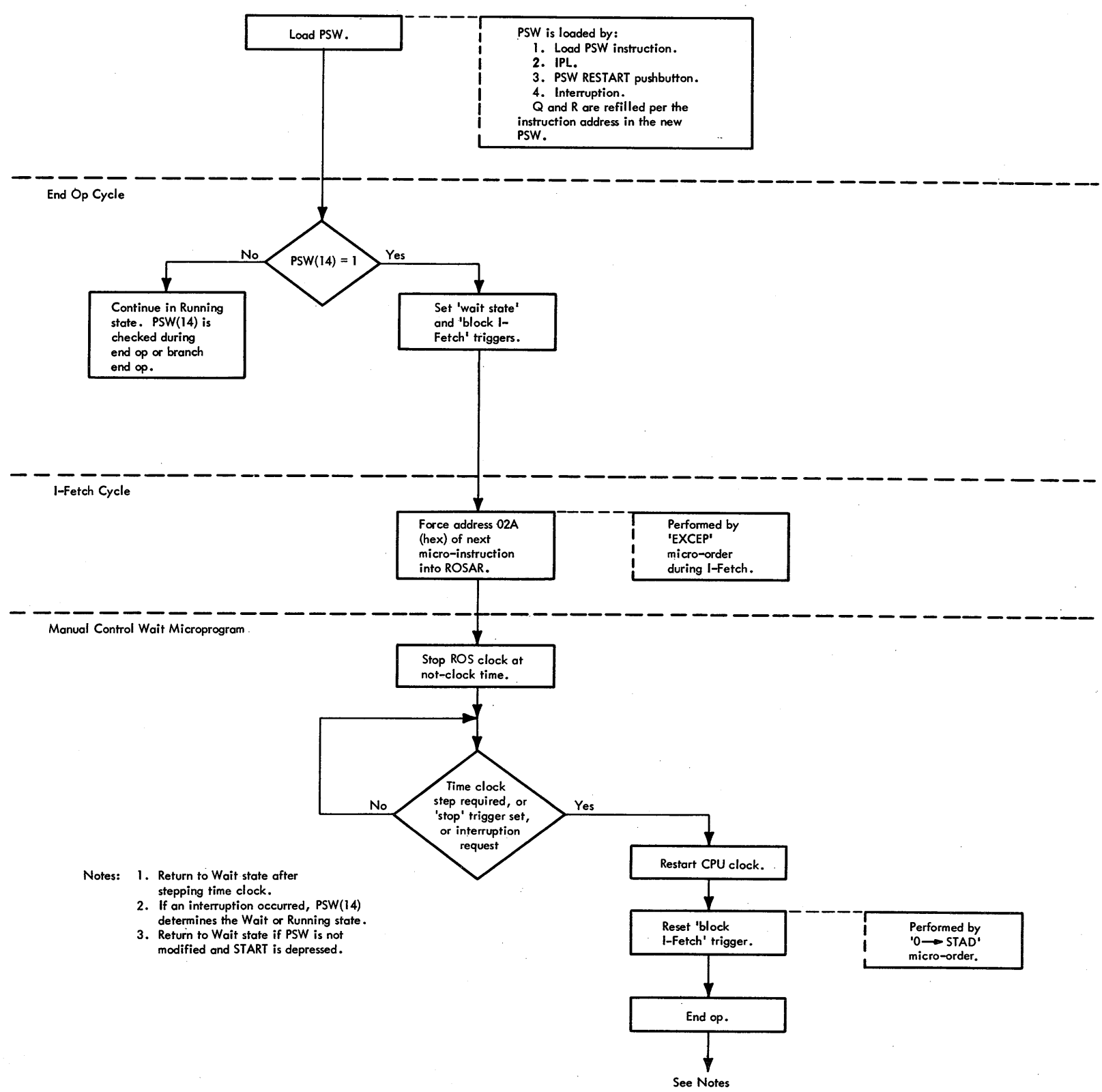


Diagram 6-20. Wait State Microprogram Routine

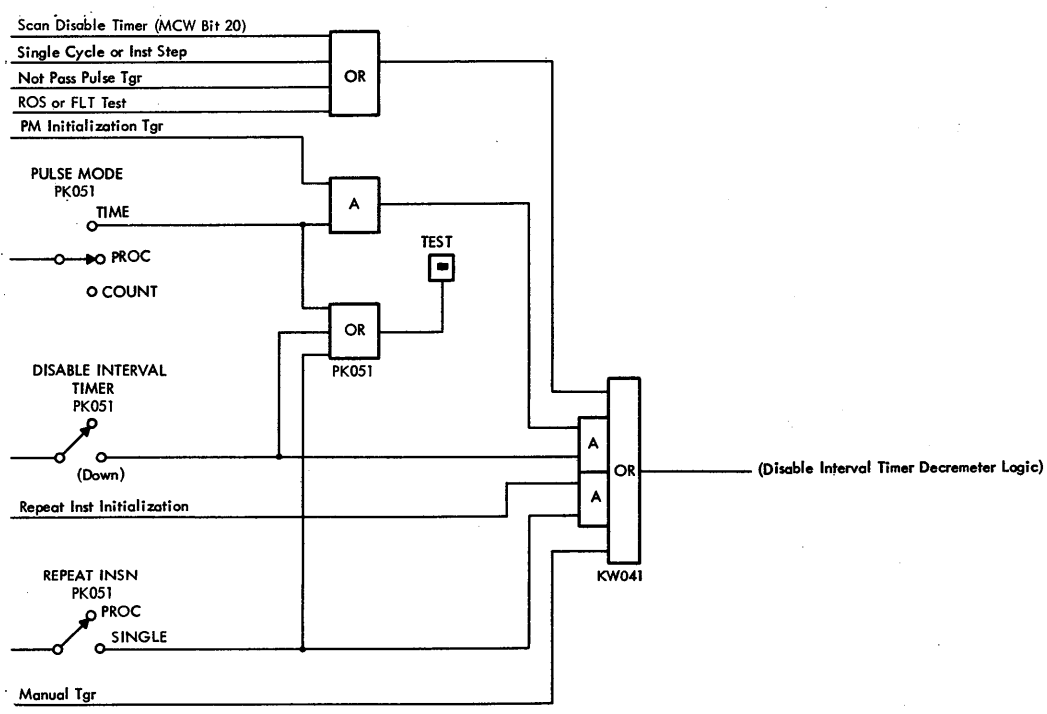


Diagram 6-21. Disable Interval Timer Logic

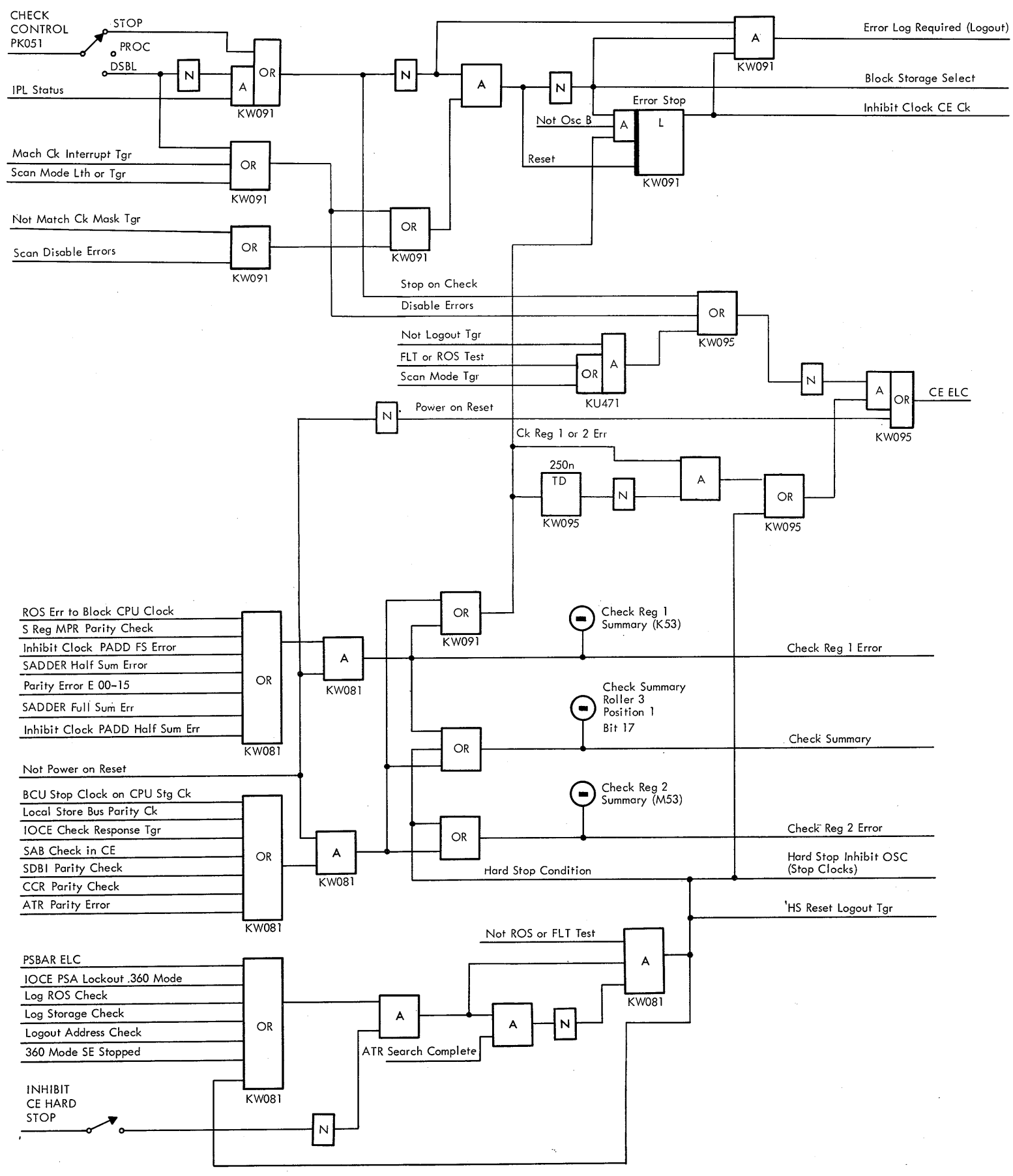


Diagram 6-22. CE Check Control and Inhibit CE Hardstop Switches, Logic and Error Controls

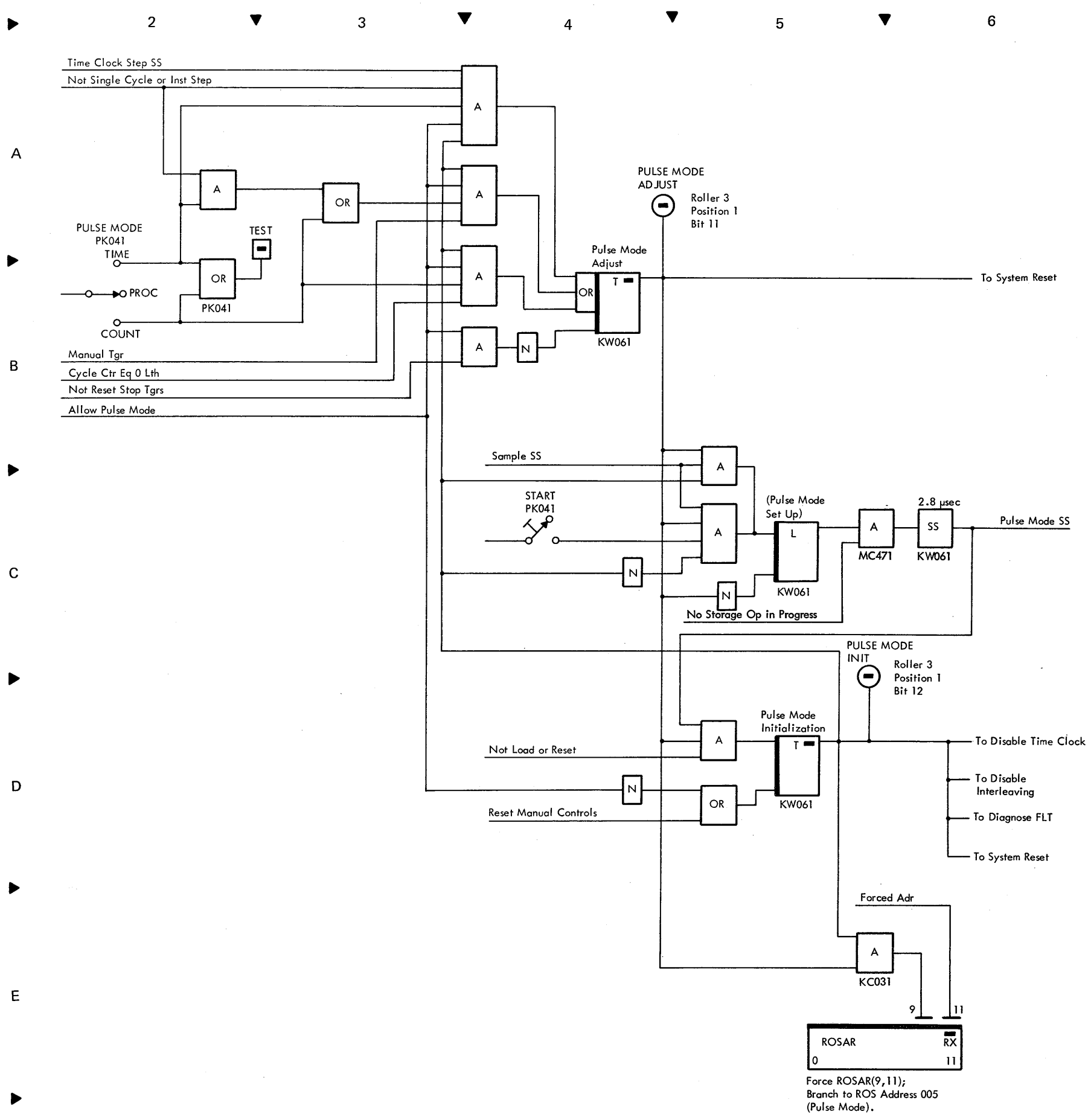
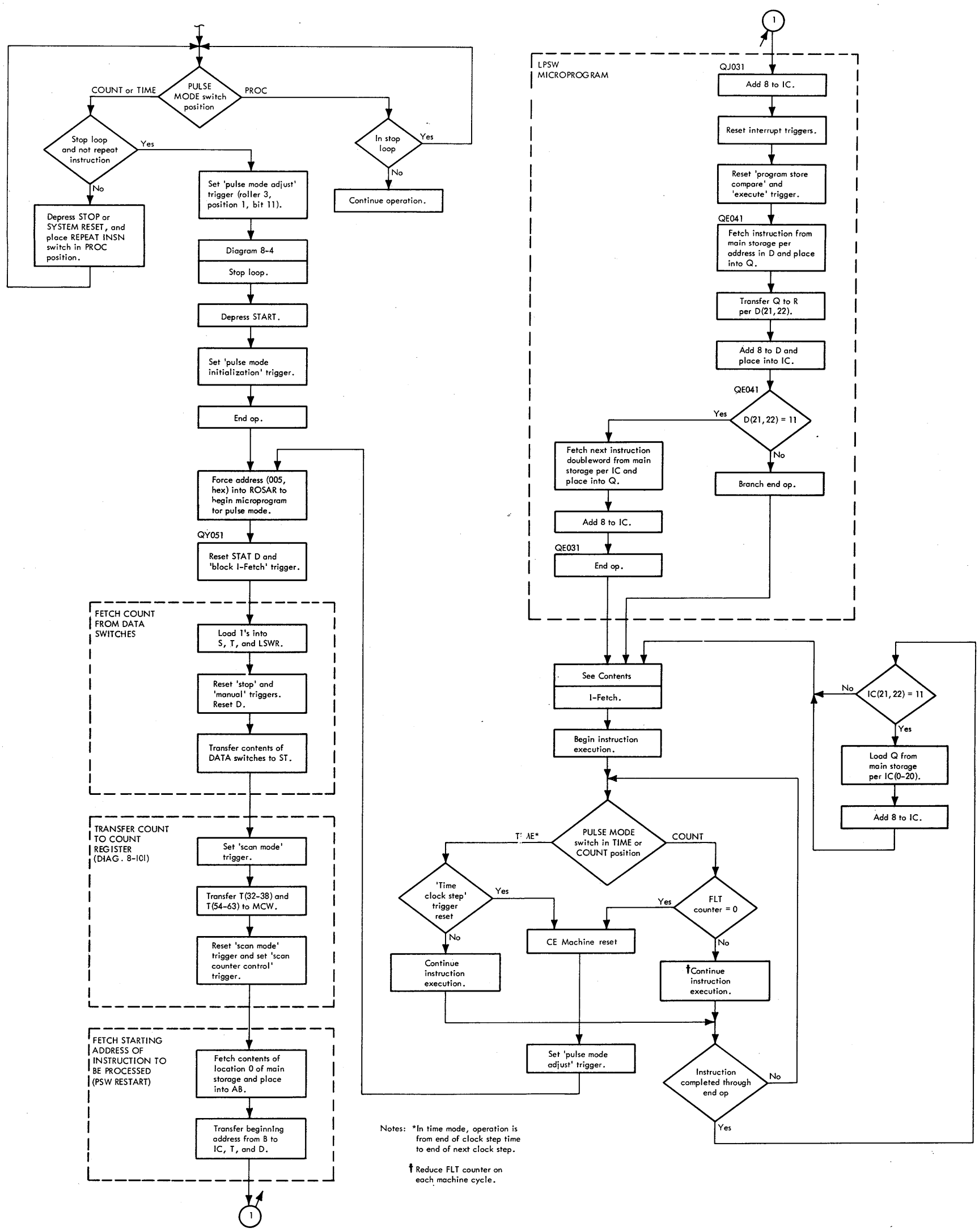


Diagram 6-23. Pulse Mode Controls



Notes: *In time mode, operation is from end of clock step time to end of next clock step.

† Reduce FLT counter on each machine cycle.

Diagram 6-24. Pulse Mode Operation

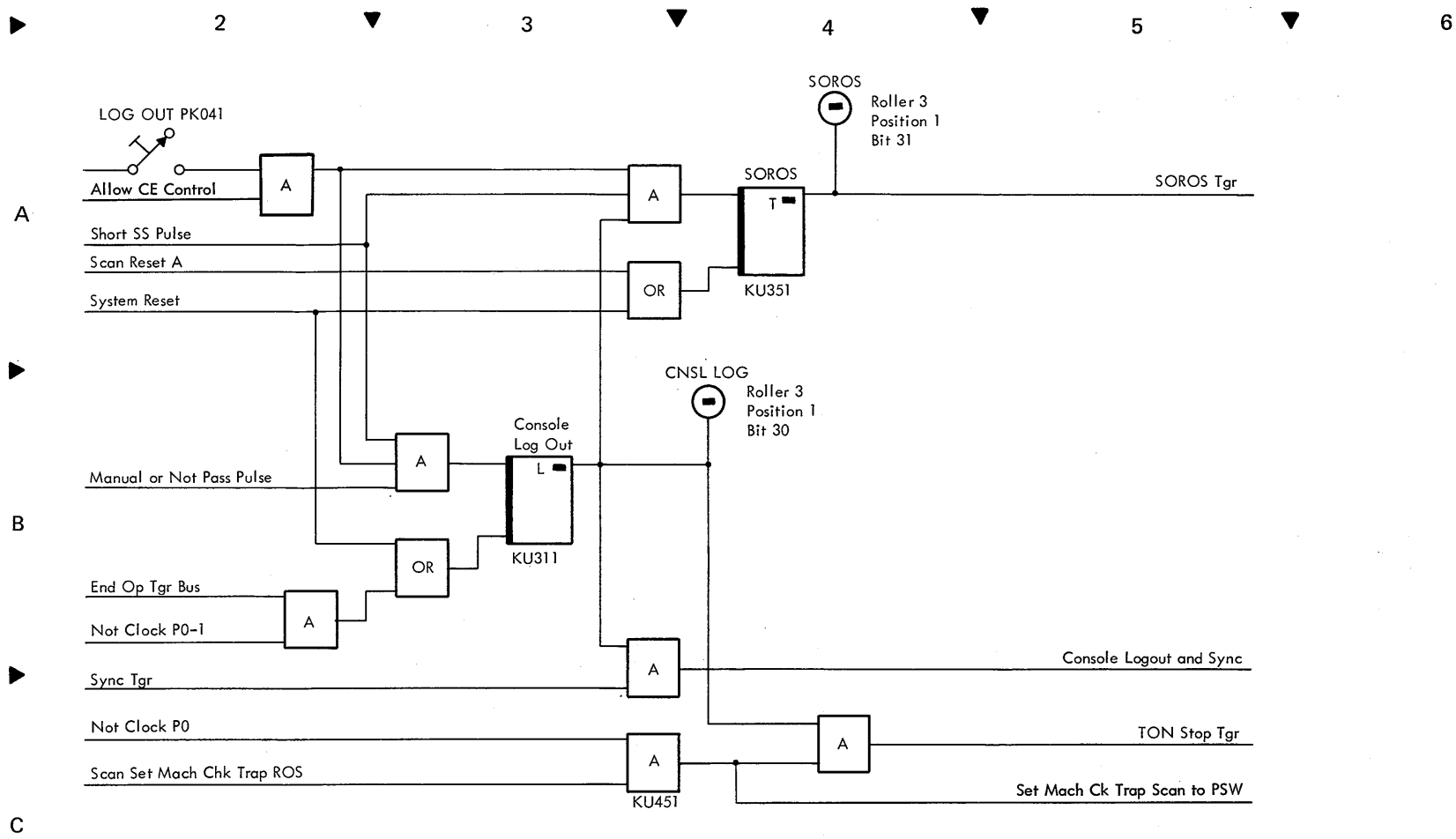


Diagram 6-25. LOG OUT Pushbutton Logic

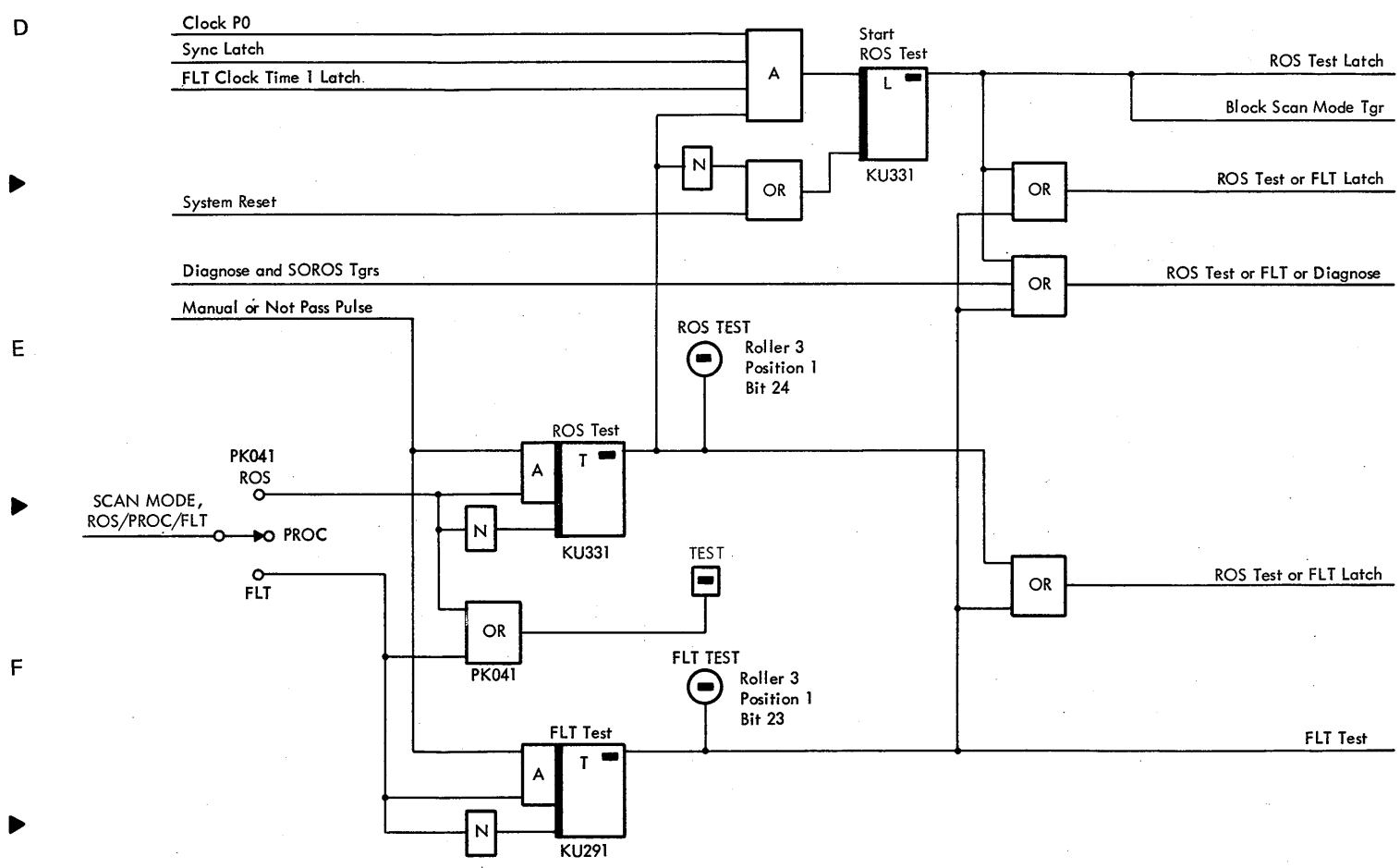


Diagram 6-26. SCAN MODE, ROS/PROC/FLT Switch Logic

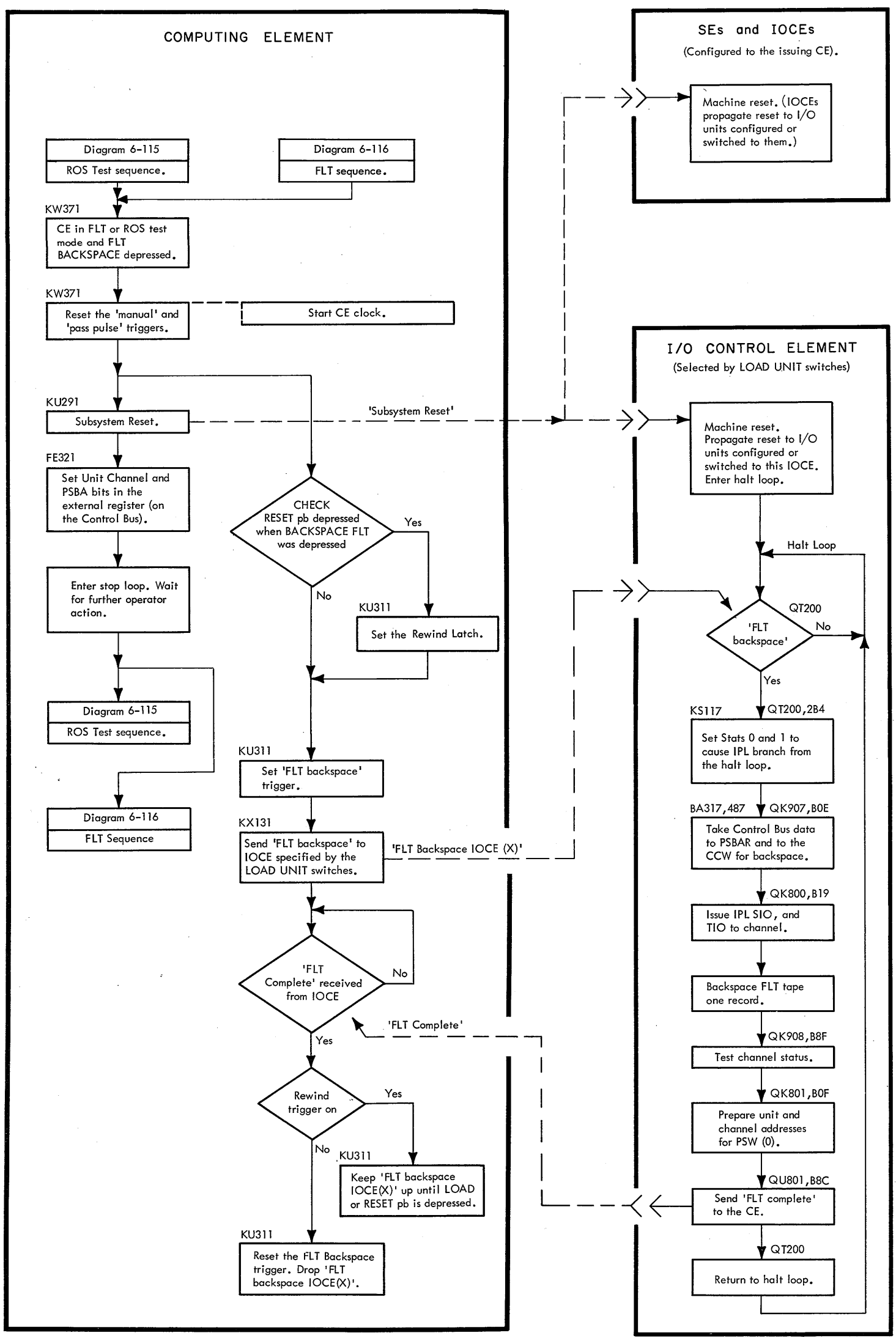


Diagram 6-27. FLT BACKSPACE Pushbutton Logic and Flow

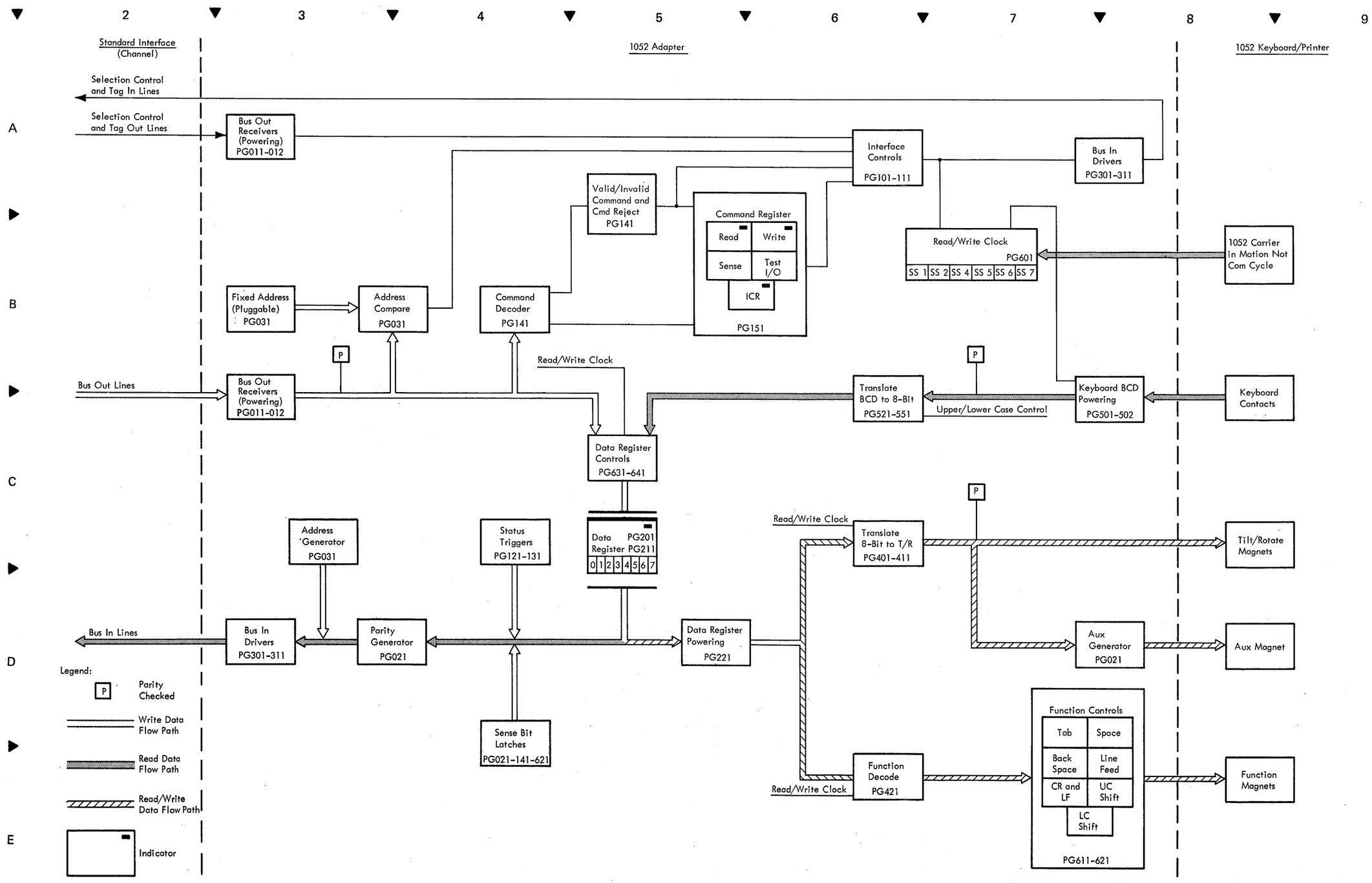
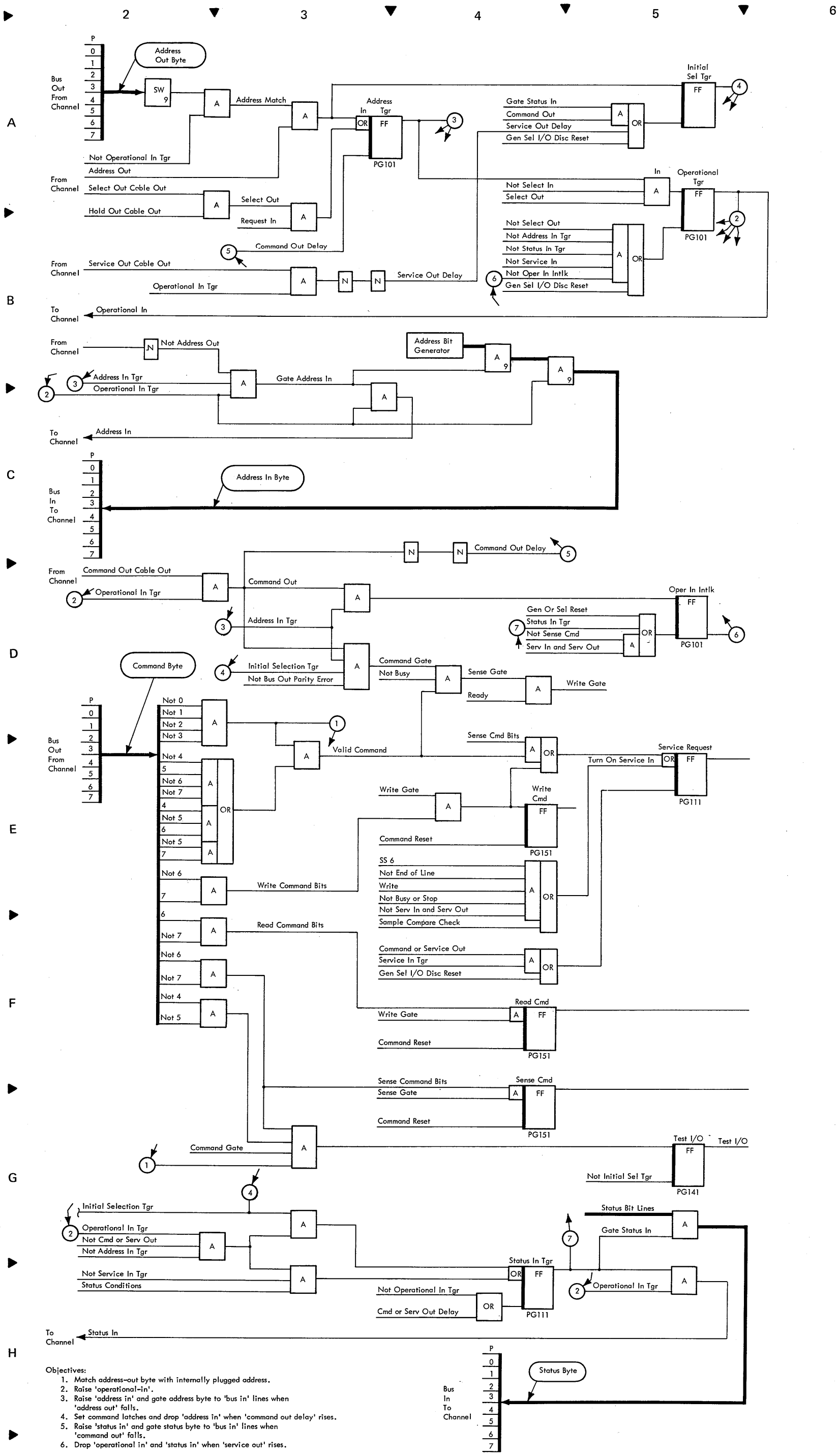


Diagram 6-28. 1052 Adapter Unit



Objectives:

1. Match address-out byte with internally plugged address.
2. Raise 'operational-in'.
3. Raise 'address in' and gate address byte to 'bus in' lines when 'address out' falls.
4. Set command latches and drop 'address in' when 'command out delay' rises.
5. Raise 'status in' and gate status byte to 'bus in' lines when 'command out' falls.
6. Drop 'operational in' and 'status in' when 'service out' rises.

Diagram 6-29. 1052 Adapter Initial Selection – Read, Write, Sense

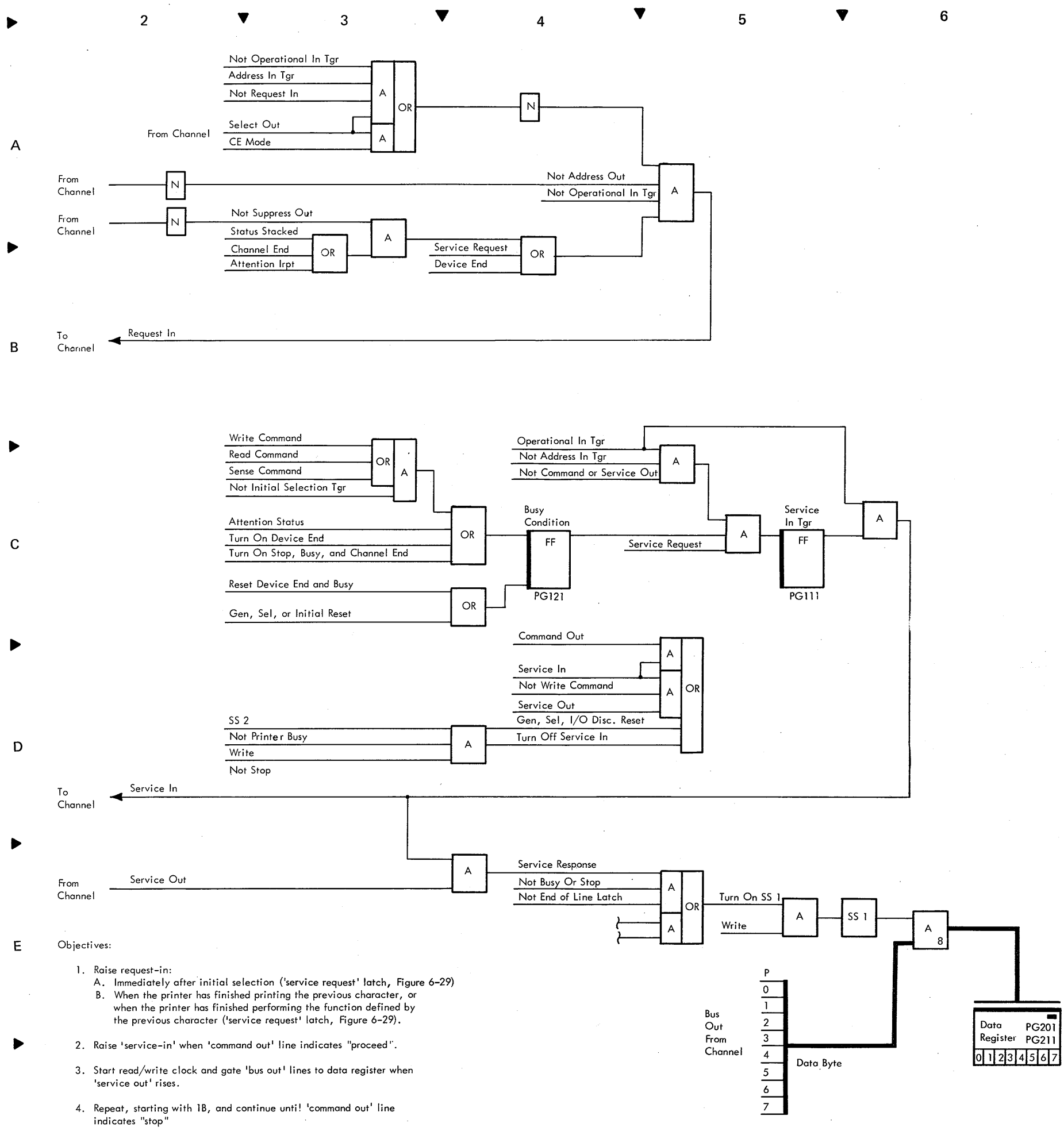
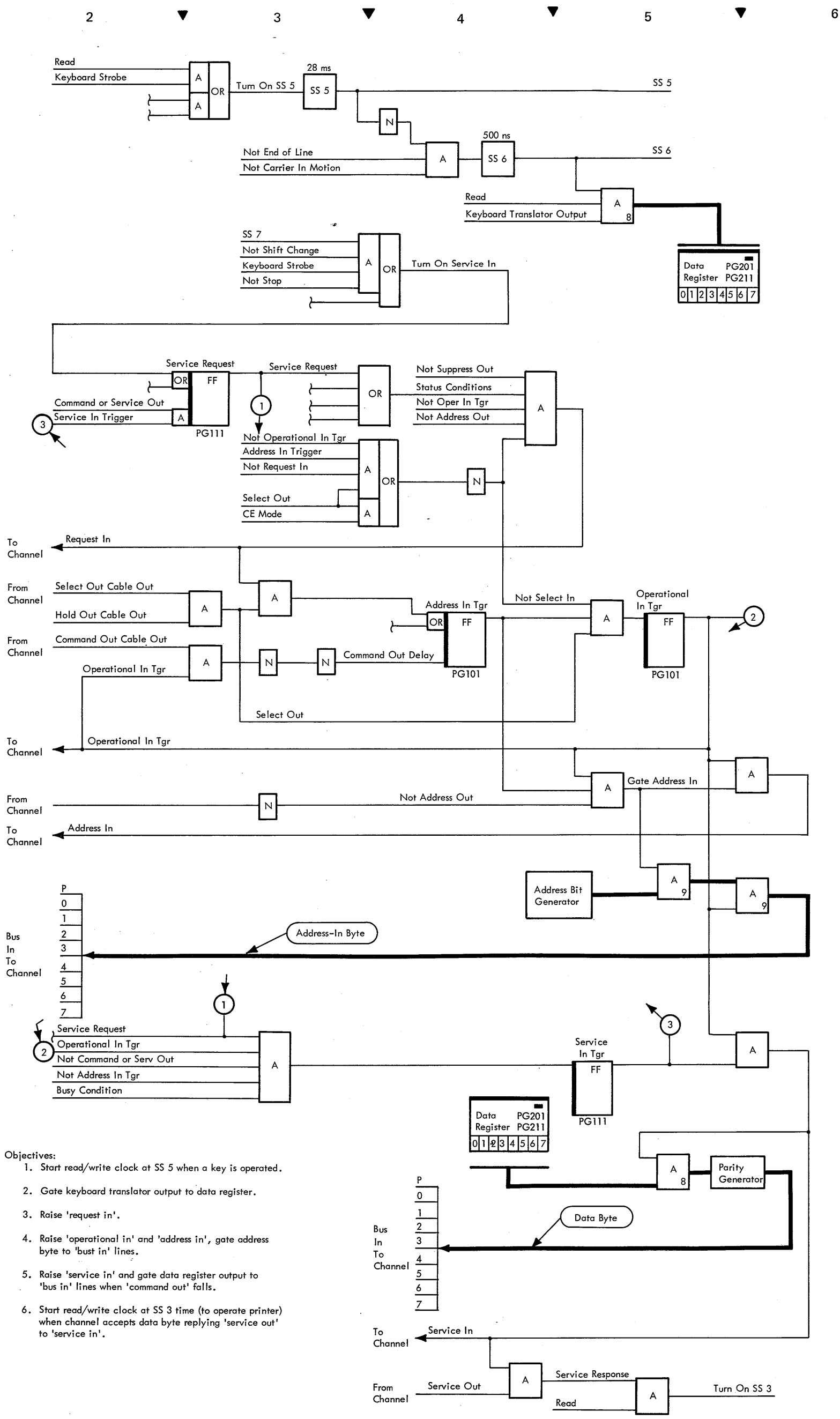


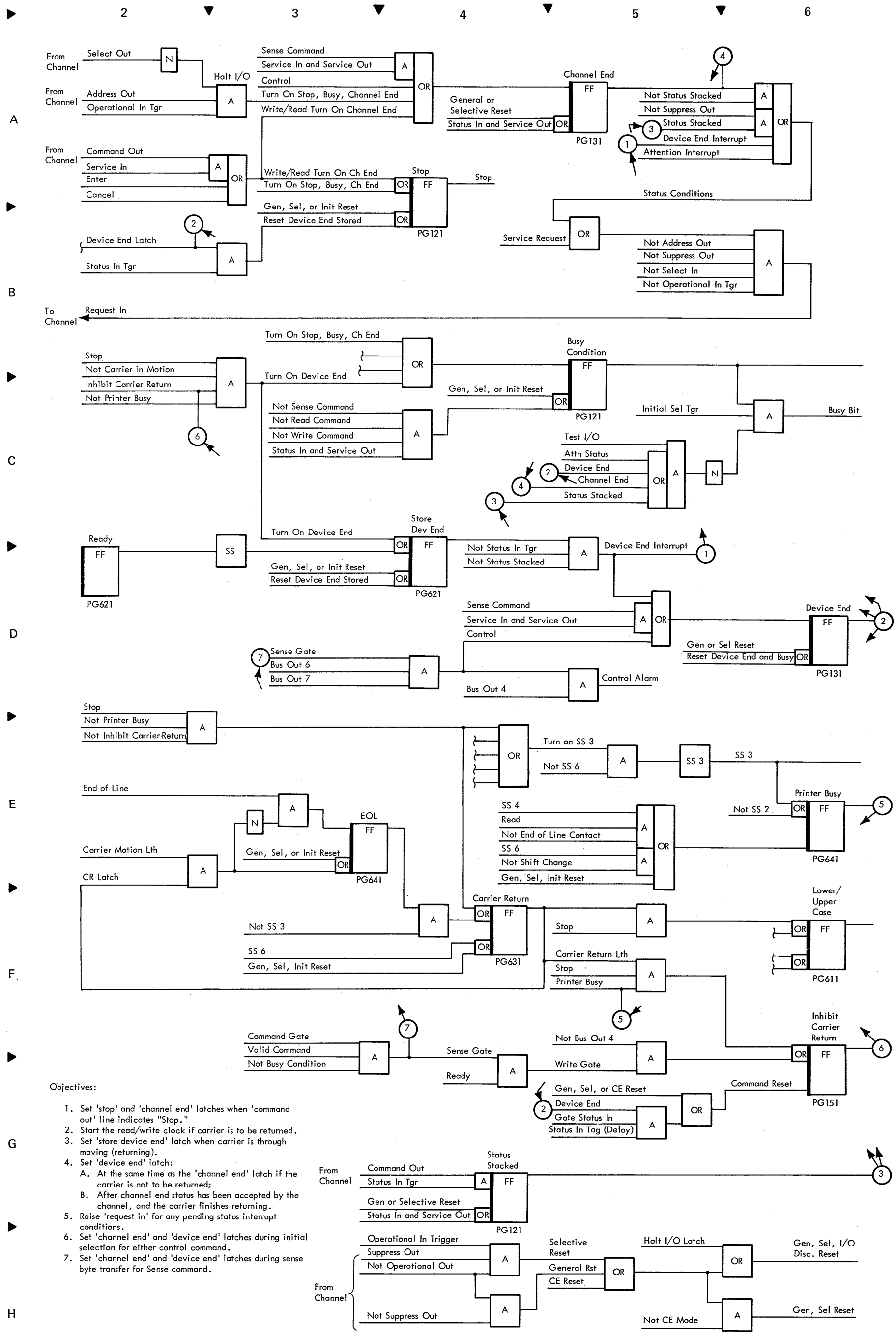
Diagram 6-30. 1052 Adapter Data Transfer – Write



Objectives:

1. Start read/write clock at SS 5 when a key is operated.
2. Gate keyboard translator output to data register.
3. Raise 'request in'.
4. Raise 'operational in' and 'address in', gate address byte to 'bust in' lines.
5. Raise 'service in' and gate data register output to 'bus in' lines when 'command out' falls.
6. Start read/write clock at SS 3 time (to operate printer) when channel accepts data byte replying 'service out' to 'service in'.

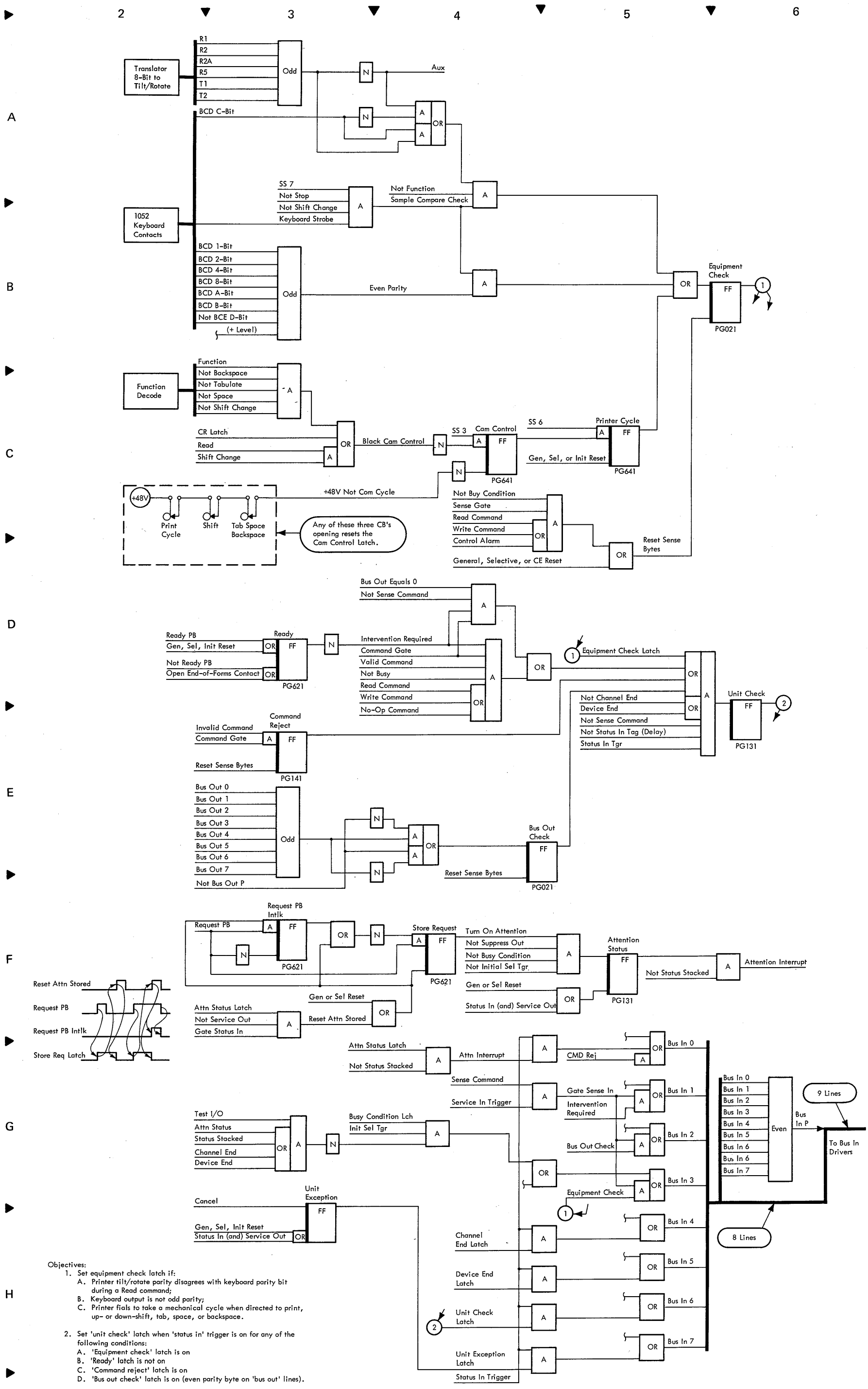
Diagram 6-31. 1052 Adapter Data Transfer – Read



Objectives:

1. Set 'stop' and 'channel end' latches when 'command out' line indicates "Stop."
2. Start the read/write clock if carrier is to be returned.
3. Set 'store device end' latch when carrier is through moving (returning).
4. Set 'device end' latch:
   A. At the same time as the 'channel end' latch if the carrier is not to be returned;
   B. After channel end status has been accepted by the channel, and the carrier finishes returning.
5. Raise 'request in' for any pending status interrupt conditions.
6. Set 'channel end' and 'device end' latches during initial selection for either control command.
7. Set 'channel end' and 'device end' latches during sense byte transfer for Sense command.

Diagram 6-32. 1052 Adapter Ending Sequence



Objectives:

1. Set equipment check latch if:
   A. Printer tilt/rotate parity disagrees with keyboard parity bit during a Read command;
   B. Keyboard output is not odd parity;
   C. Printer fials to take a mechanical cycle when directed to print, up- or down-shift, tab, space, or backspace.

2. Set 'unit check' latch when 'status in' trigger is on for any of the following conditions:
   A. 'Equipment check' latch is on
   B. 'Ready' latch is not on
   C. 'Command reject' latch is on
   D. 'Bus out check' latch is on (even parity byte on 'bus out' lines).

Diagram 6-33. 1052 Adapter Sense and Status Bytes

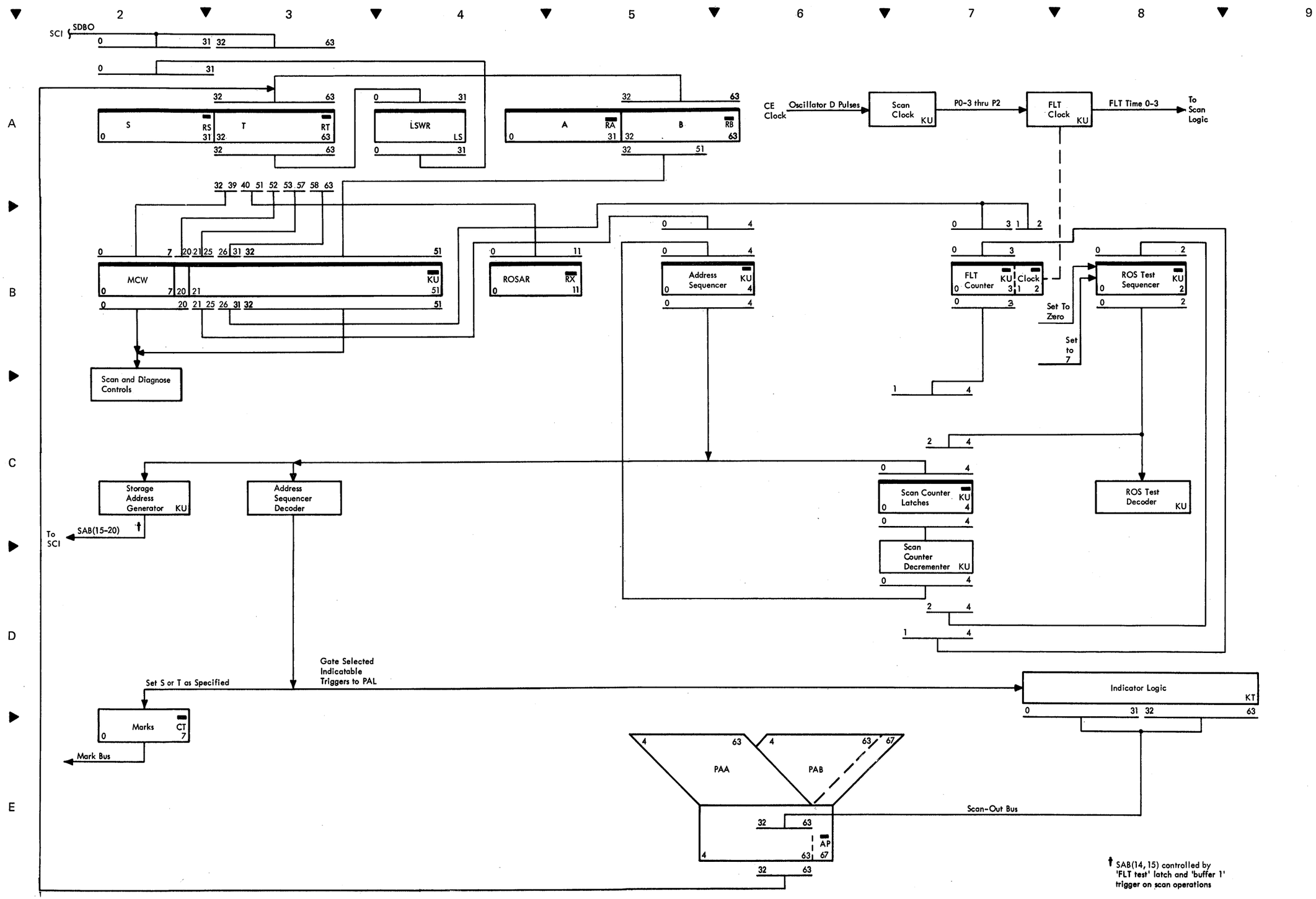


Diagram 6-101. Scan Data and Control

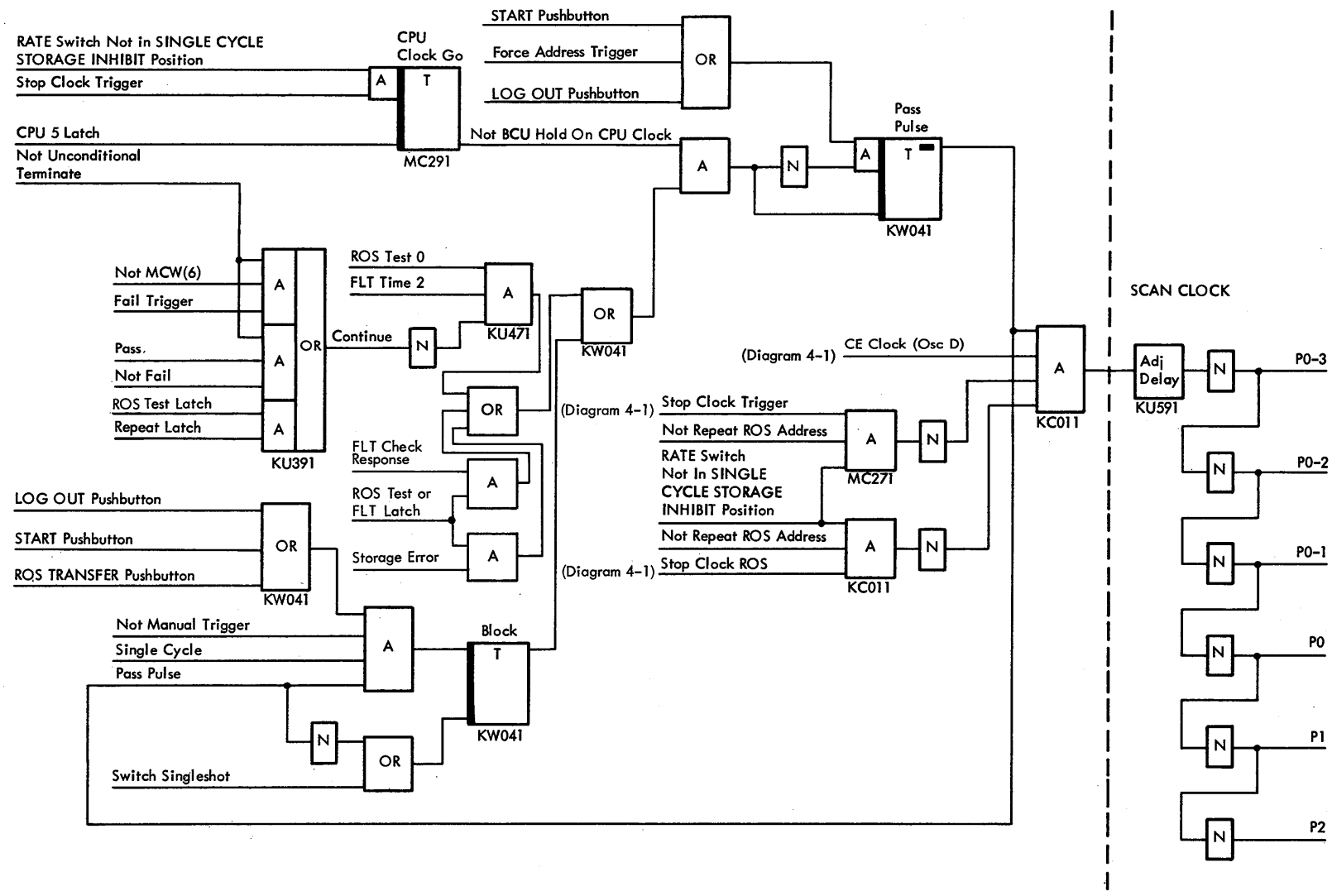
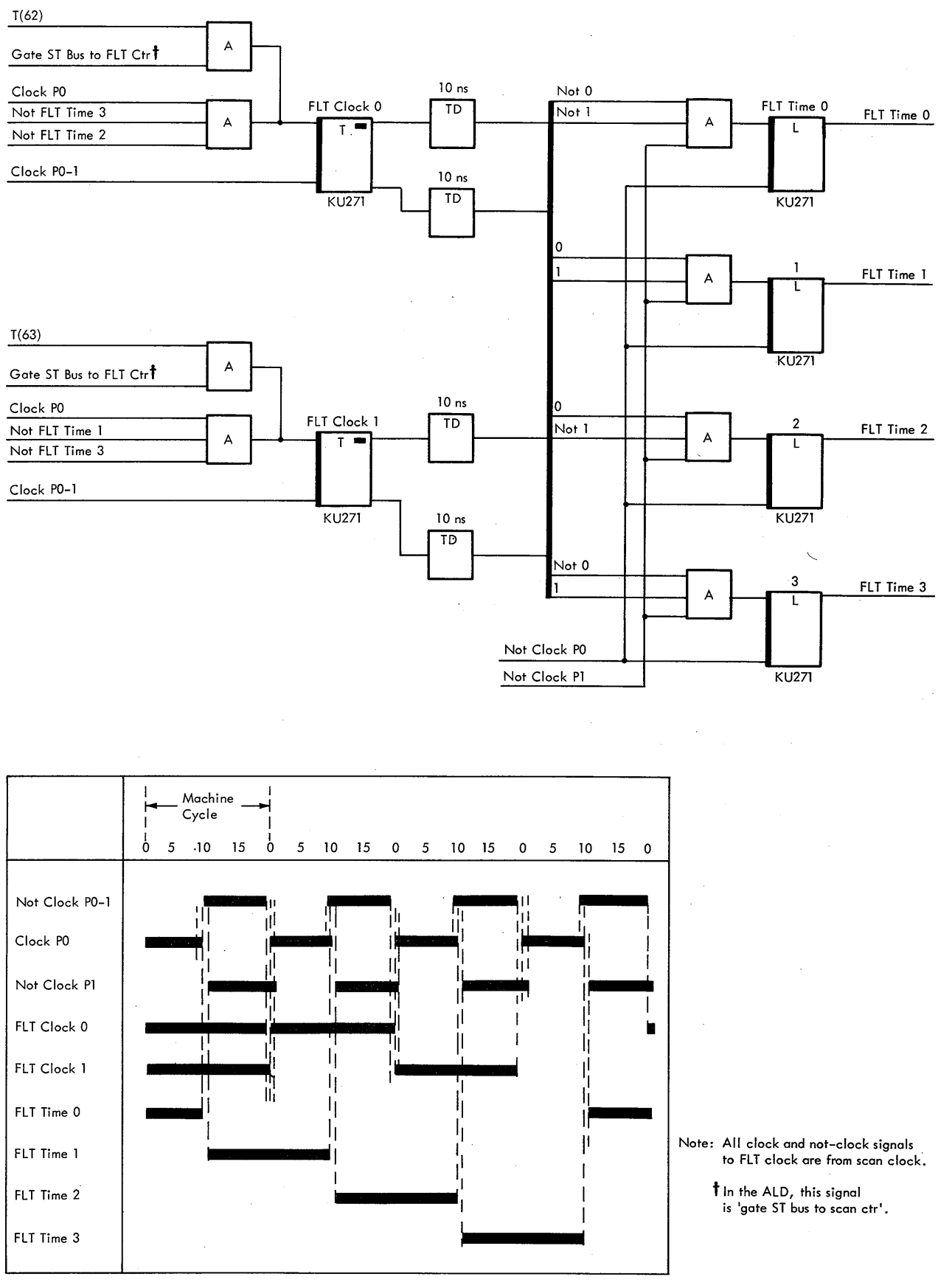


Diagram 6-102. Scan Clock



Note: All clock and not-clock signals to FLT clock are from scan clock.

† In the ALD, this signal is 'gate ST bus to scan ctr'.

Diagram 6-103. FLT Clock

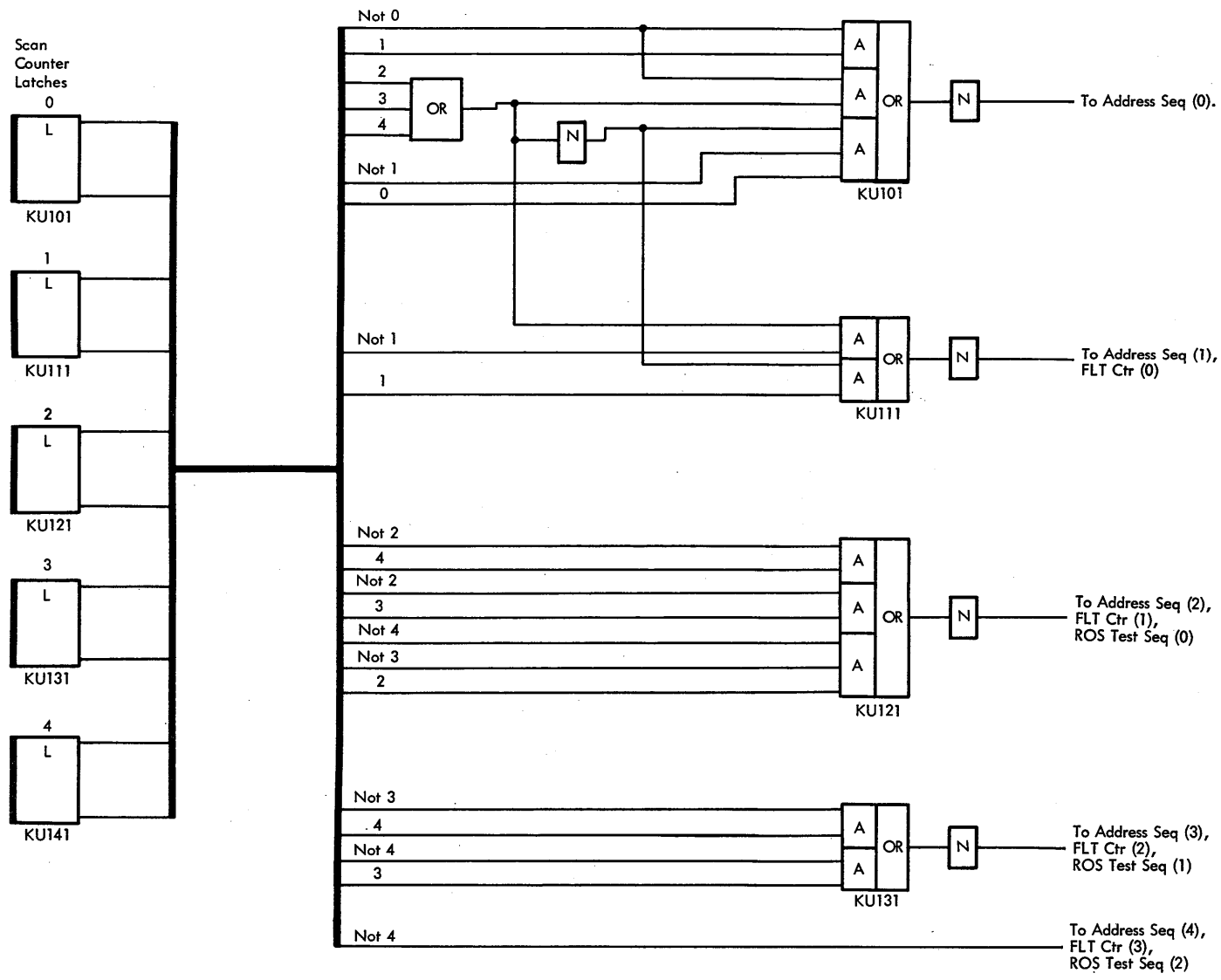
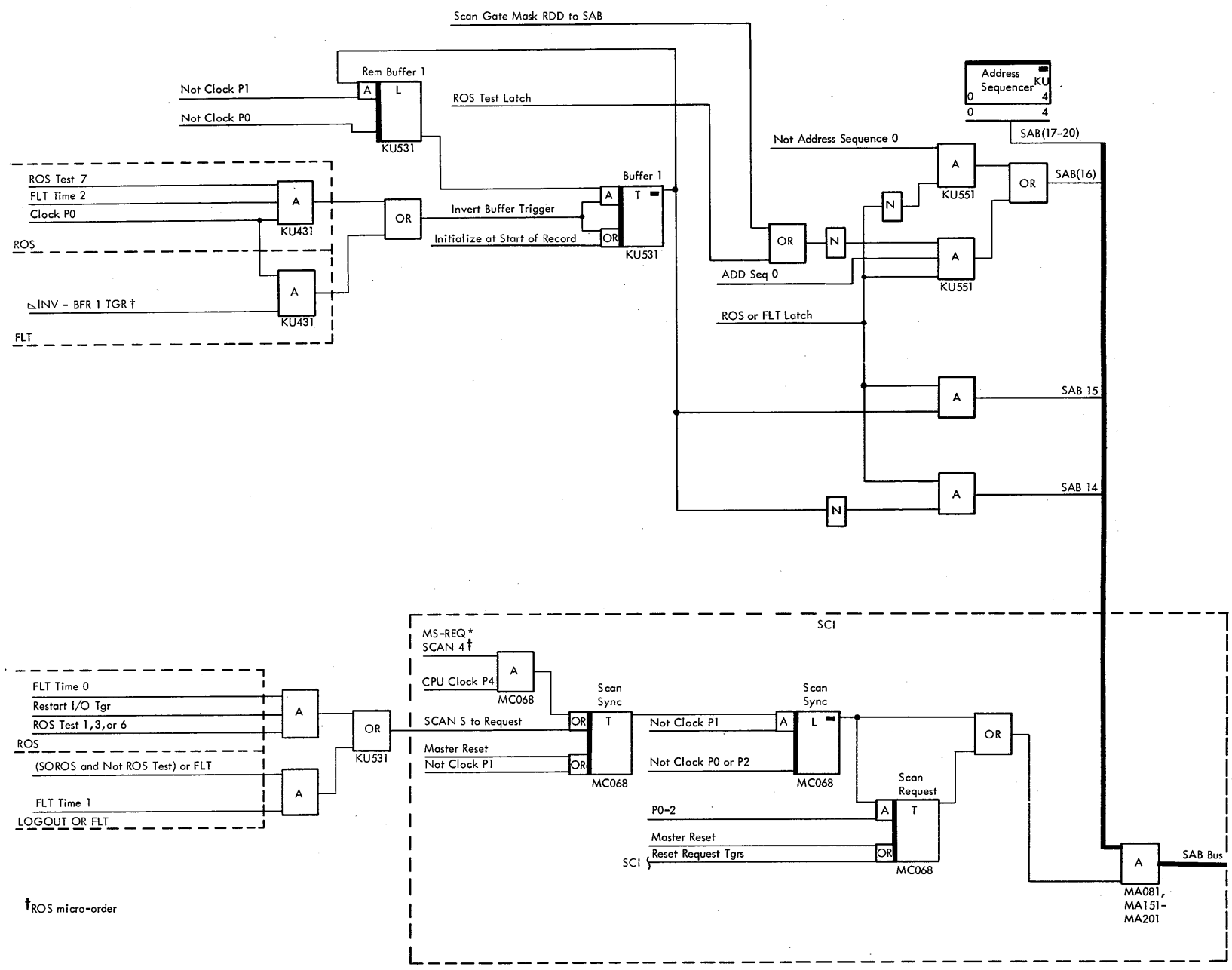


Diagram 6-104. Scan Counter Latches and Decrementer



SAB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Logout 80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Logout F8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
Logout 100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Logout 138	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0
Buffer 1:																								
FLT's 100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
FLT's 180	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
Buffer 2:																								
FLT's 200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
FLT's 280	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Not Address Sequence 0 — Address Sequencer — OFF ON — Buffer 1 Trigger — Address Sequencer

Note: Scan-generated main storage addresses start with the highest value required and are decremented to the lowest value required.

Diagram 6-105. Scan Storage Address Generator

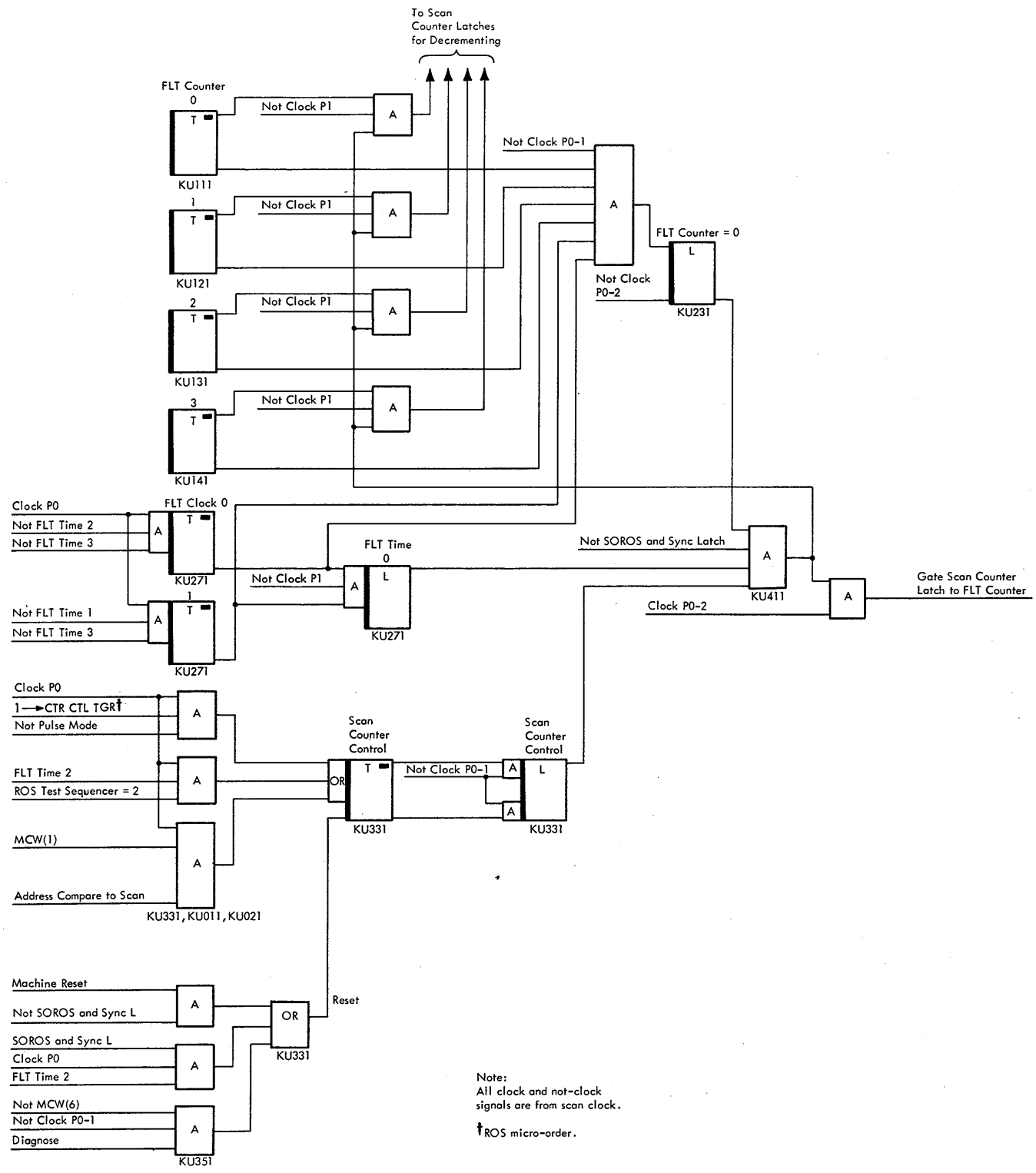


Diagram 6-106. FLT Counter Decrementing

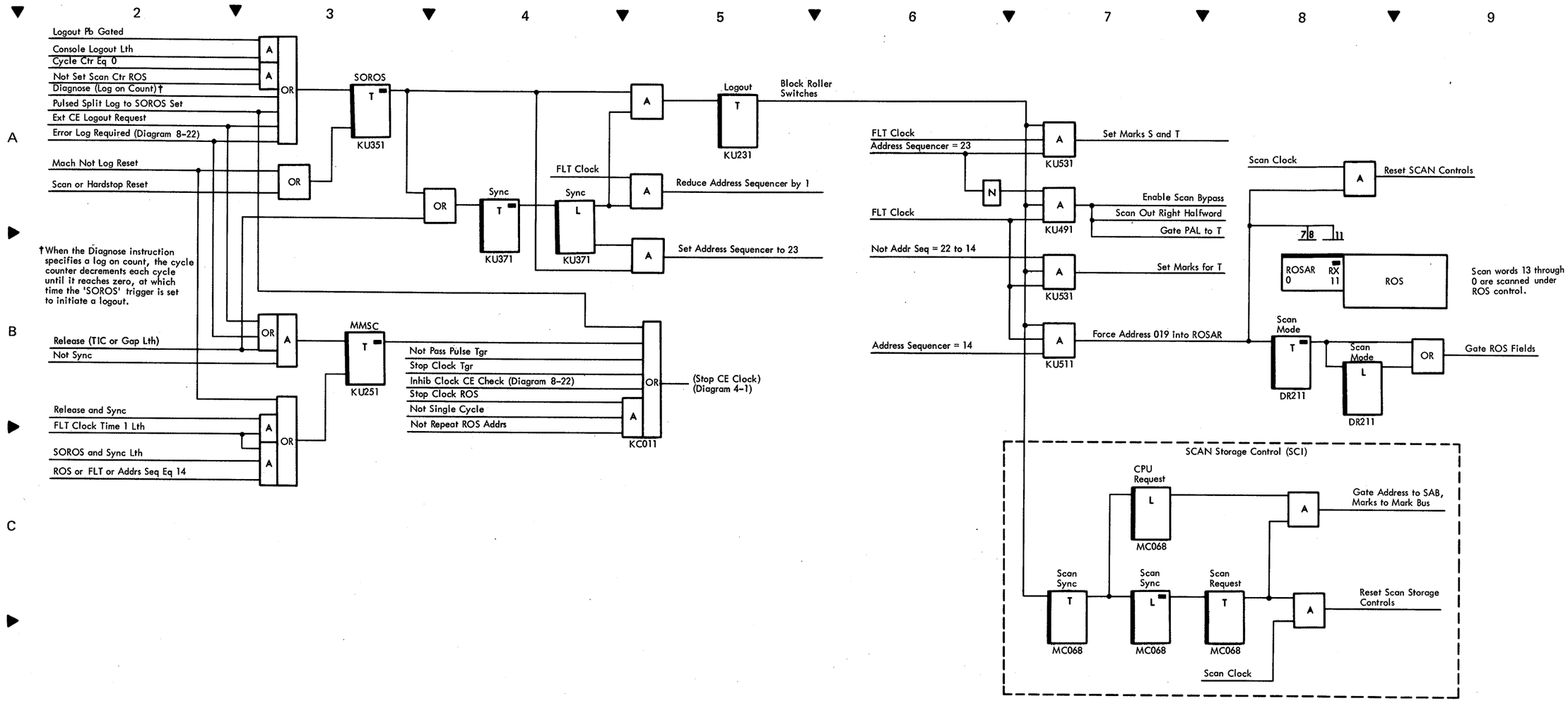
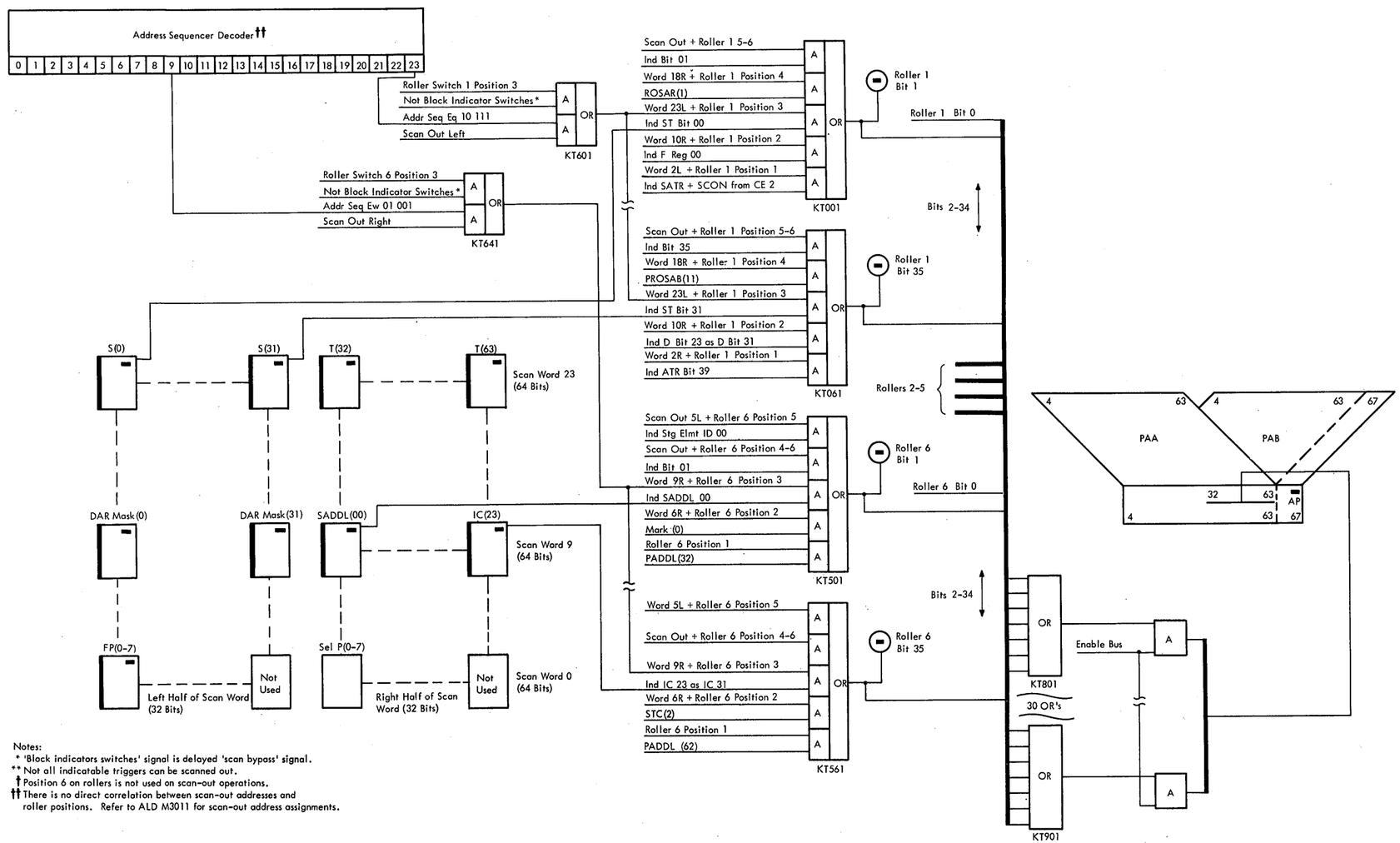


Diagram 6-108. Logout Control Logic



Notes:
* 'Block indicators switches' signal is delayed 'scan bypass' signal.
** Not all indicatable triggers can be scanned out.
† Position 6 on rollers is not used on scan-out operations.
†† There is no direct correlation between scan-out addresses and roller positions. Refer to ALD M3011 for scan-out address assignments.

Diagram 6-107. Scan-Out Bus Data Flow

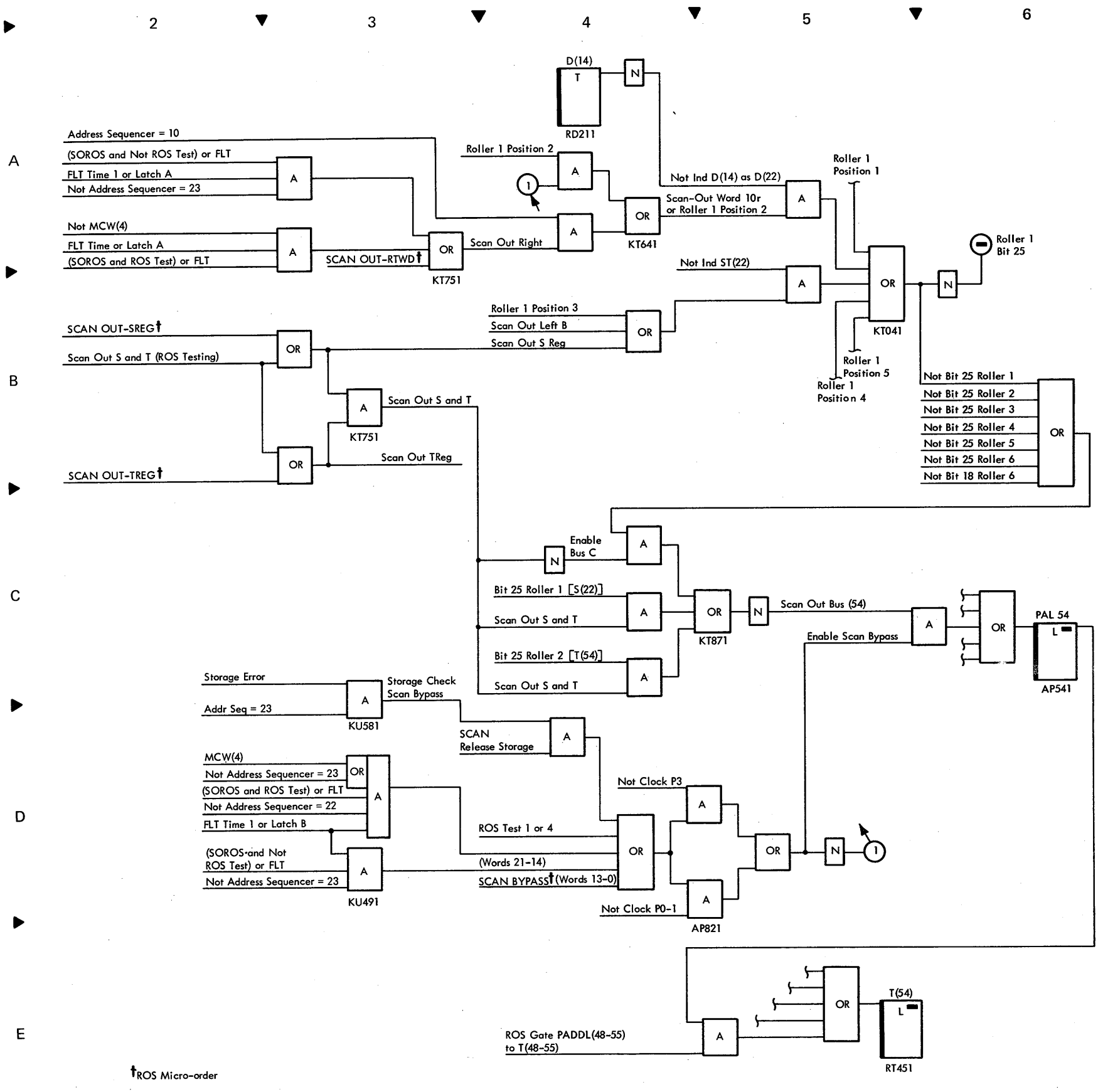


Diagram 6-109. Scan-Out Path For One Bit

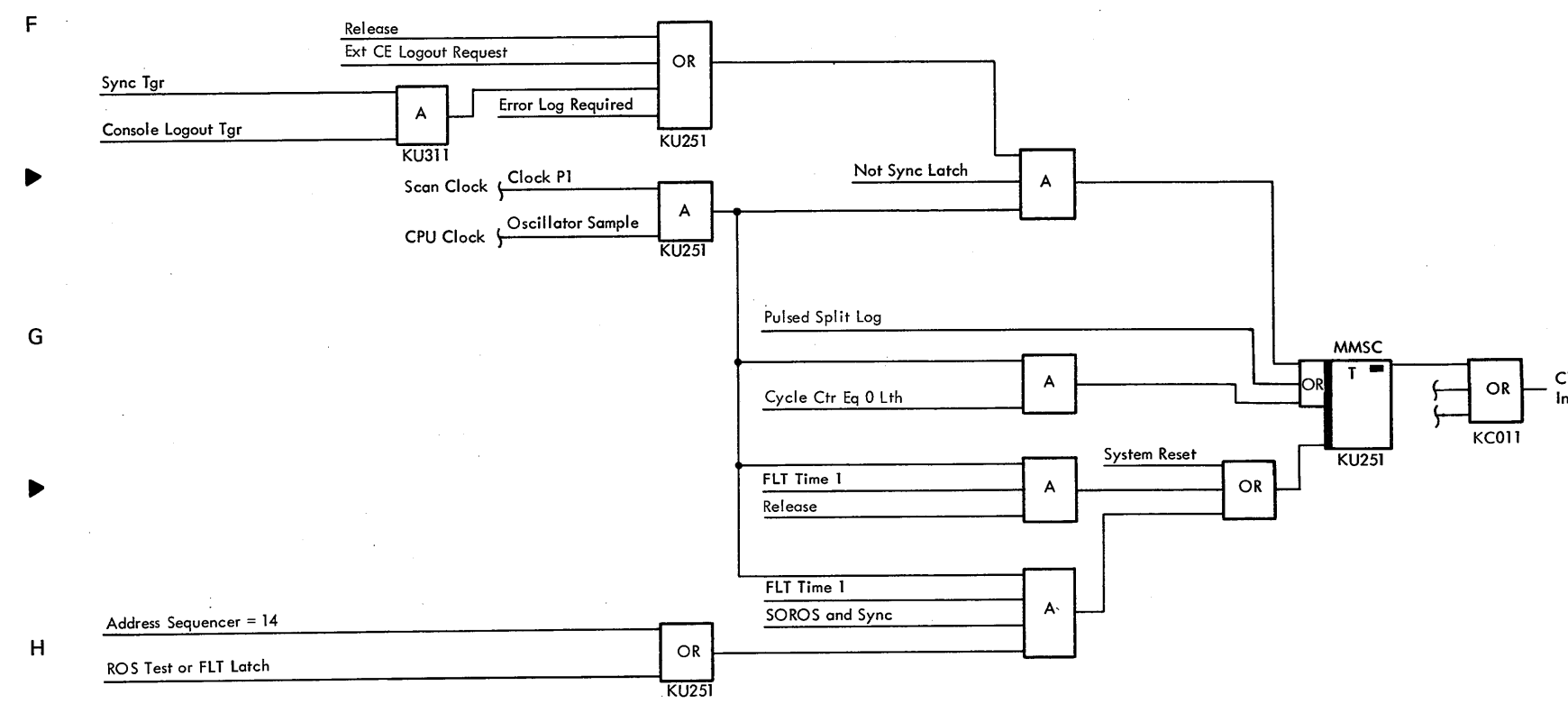
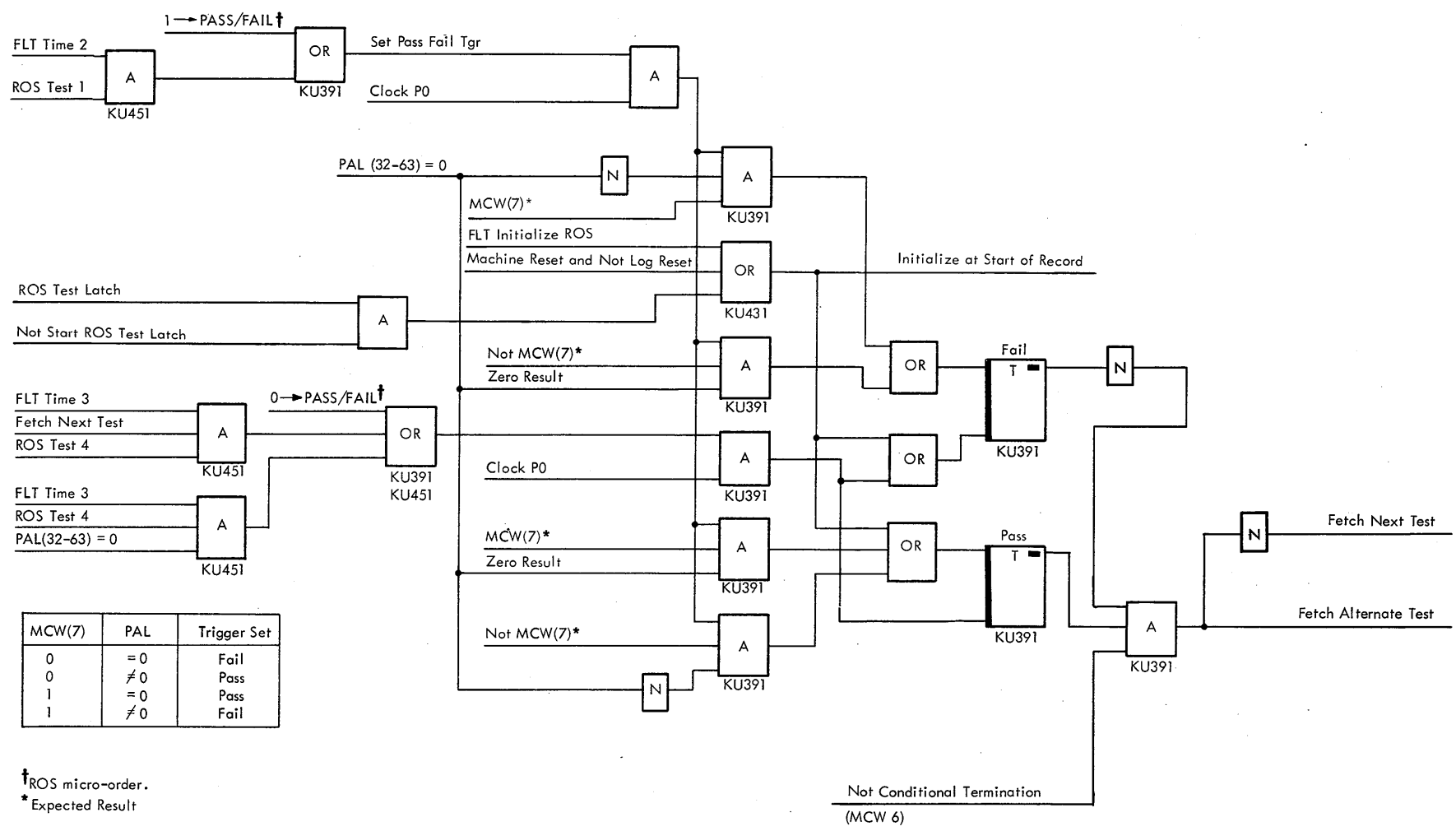


Diagram 6-110. Maintenance Mode Stop Clock Logic



MCW(7)	PAL	Trigger Set
0	= 0	Fail
0	≠ 0	Pass
1	= 0	Pass
1	≠ 0	Fail

†ROS micro-order.
*Expected Result

Diagram 6-111. Scan Control Triggers

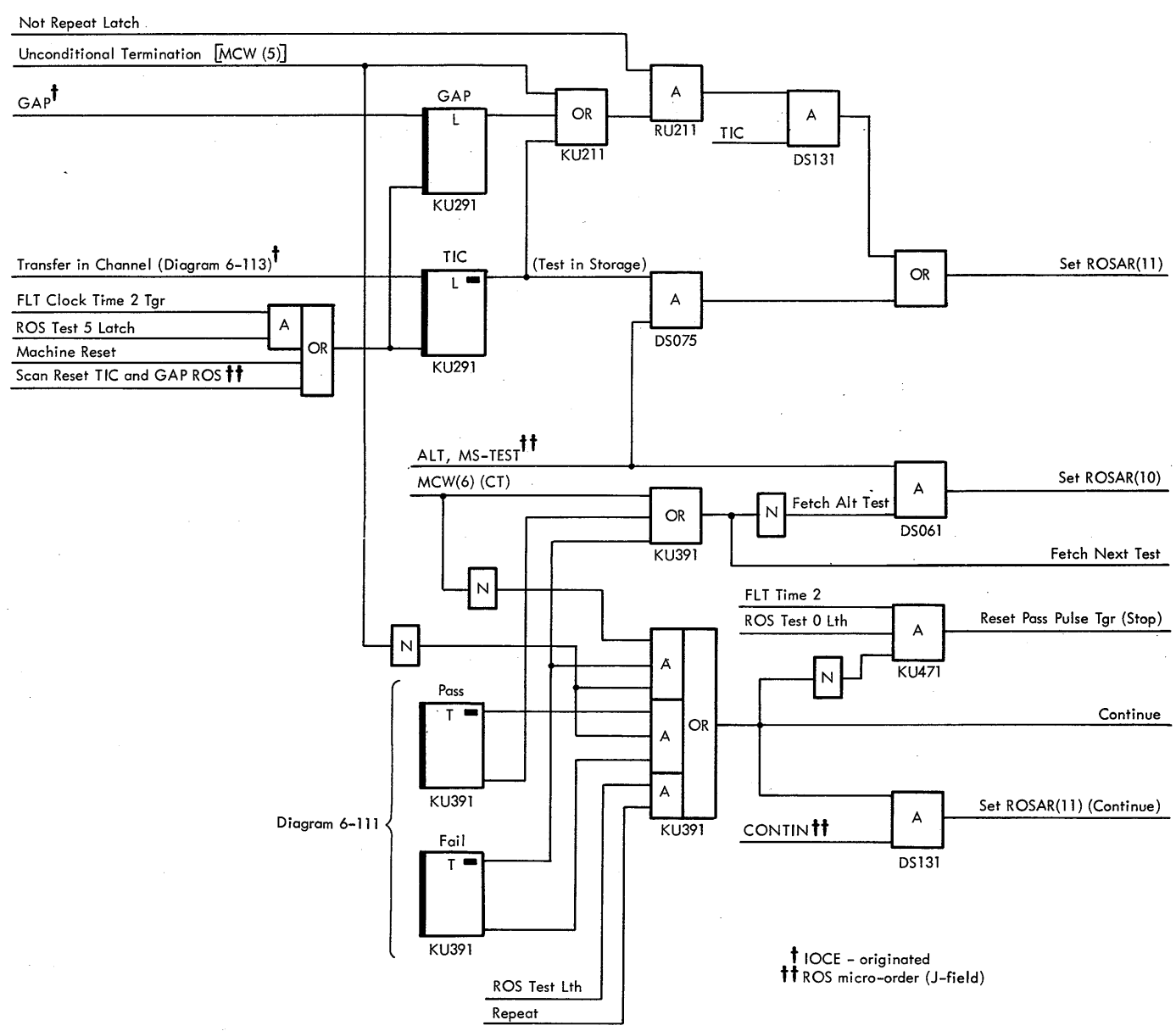


Diagram 6-112. Scan Control of ROS Microbranching

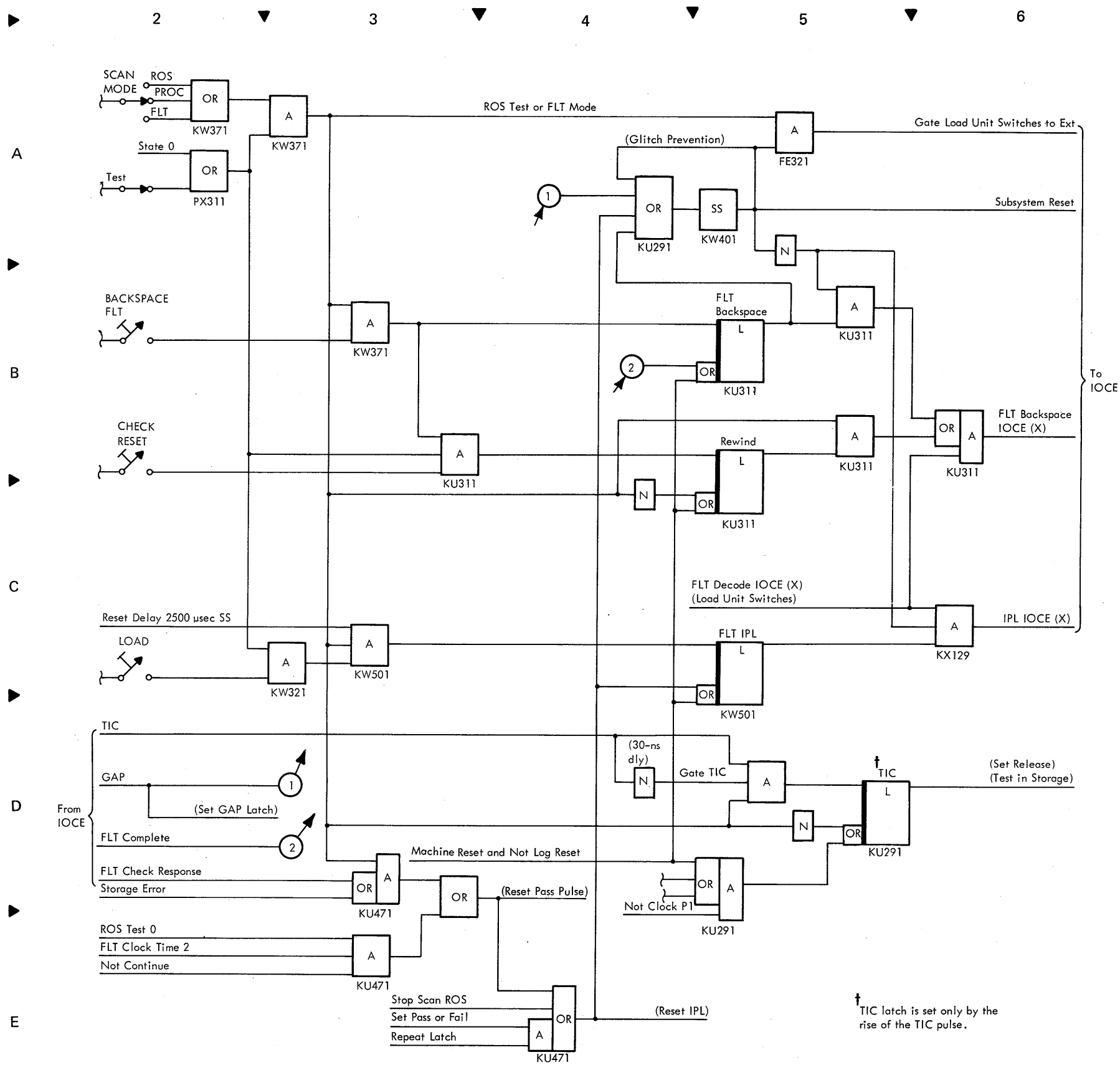


Diagram 6-113. CE Scan/IOCE Interface

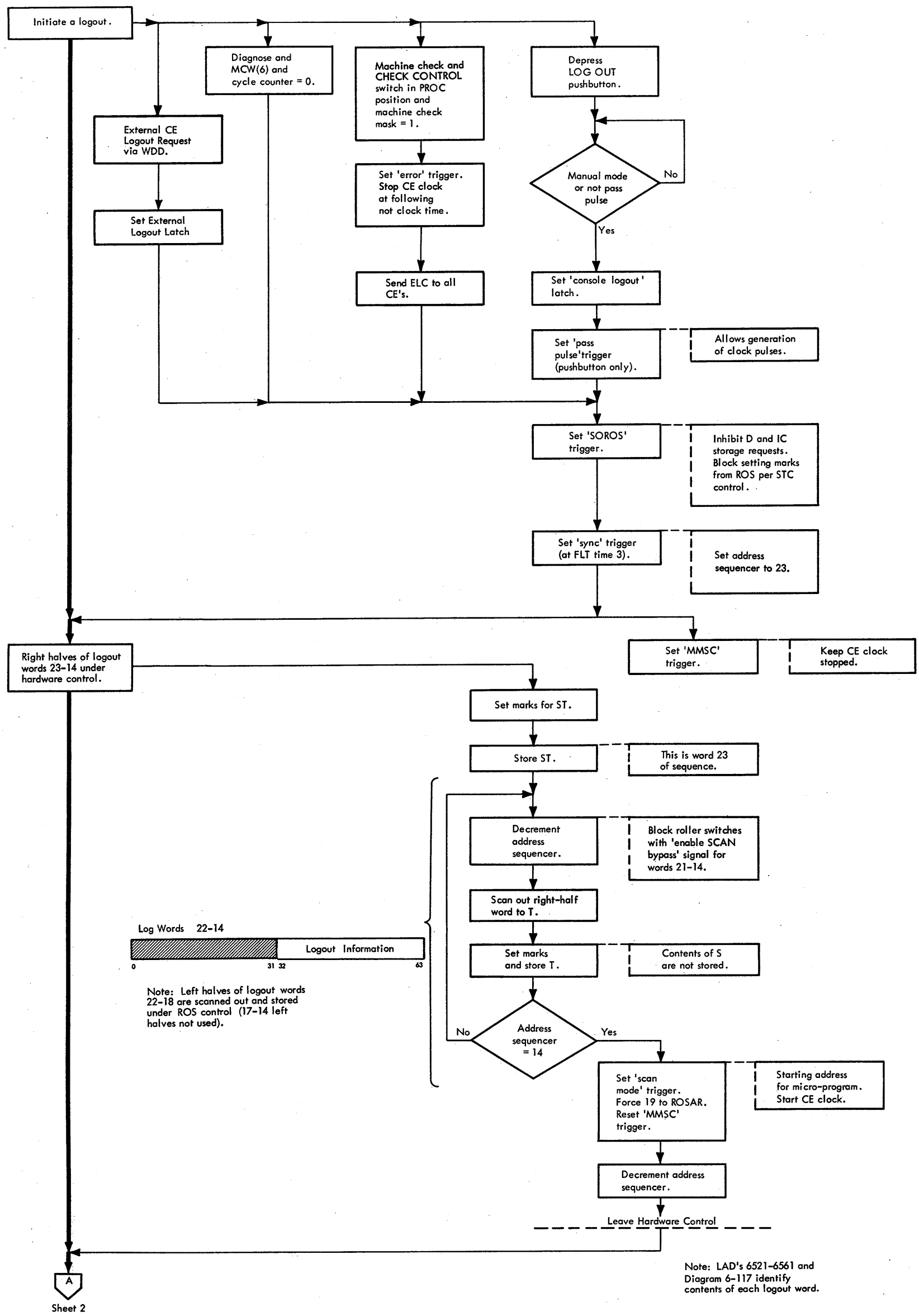


Diagram 6-114. Logout Sequence (Sheet 1 of 2)

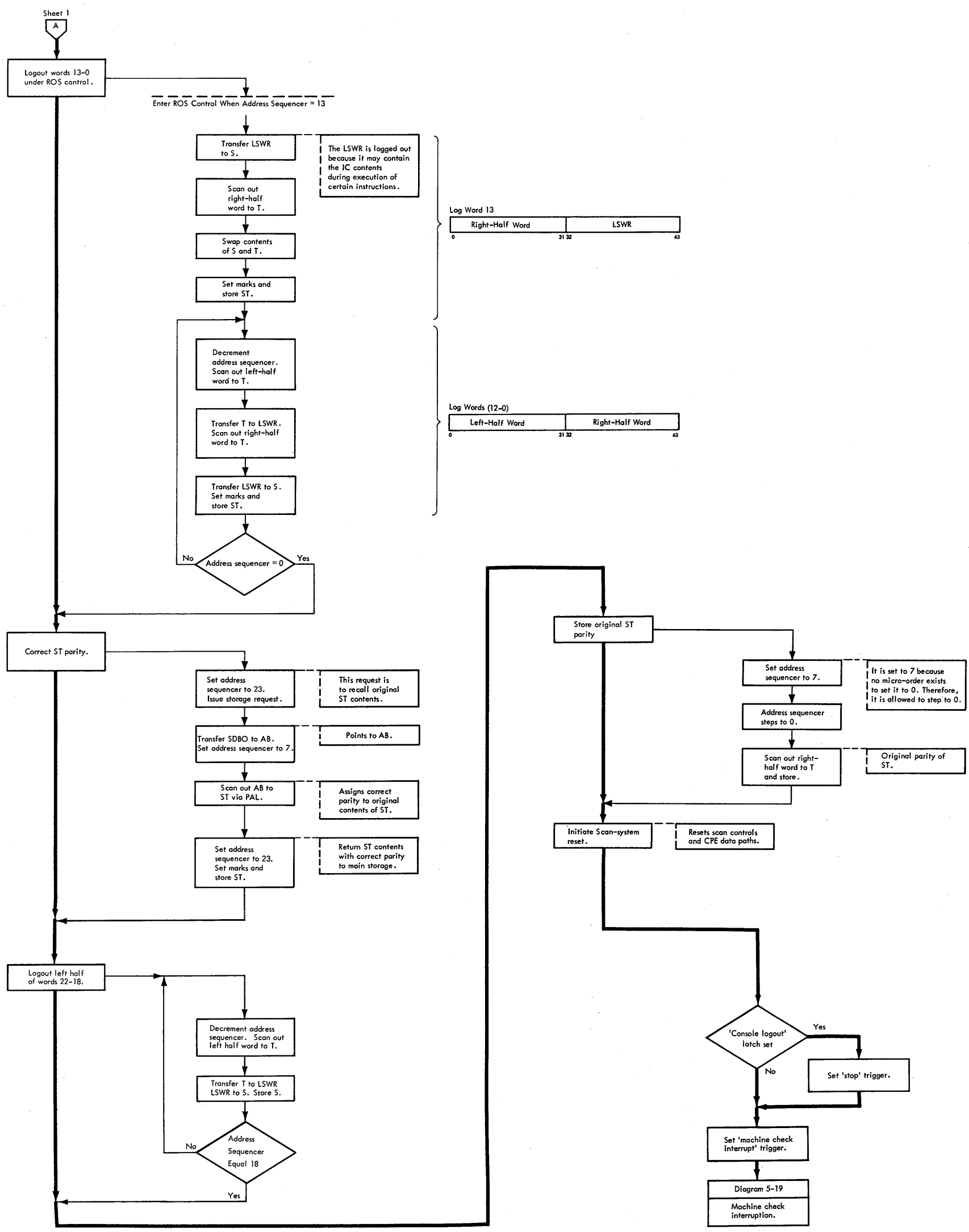


Diagram 6-114. Logout Sequence (Sheet 2 of 2)

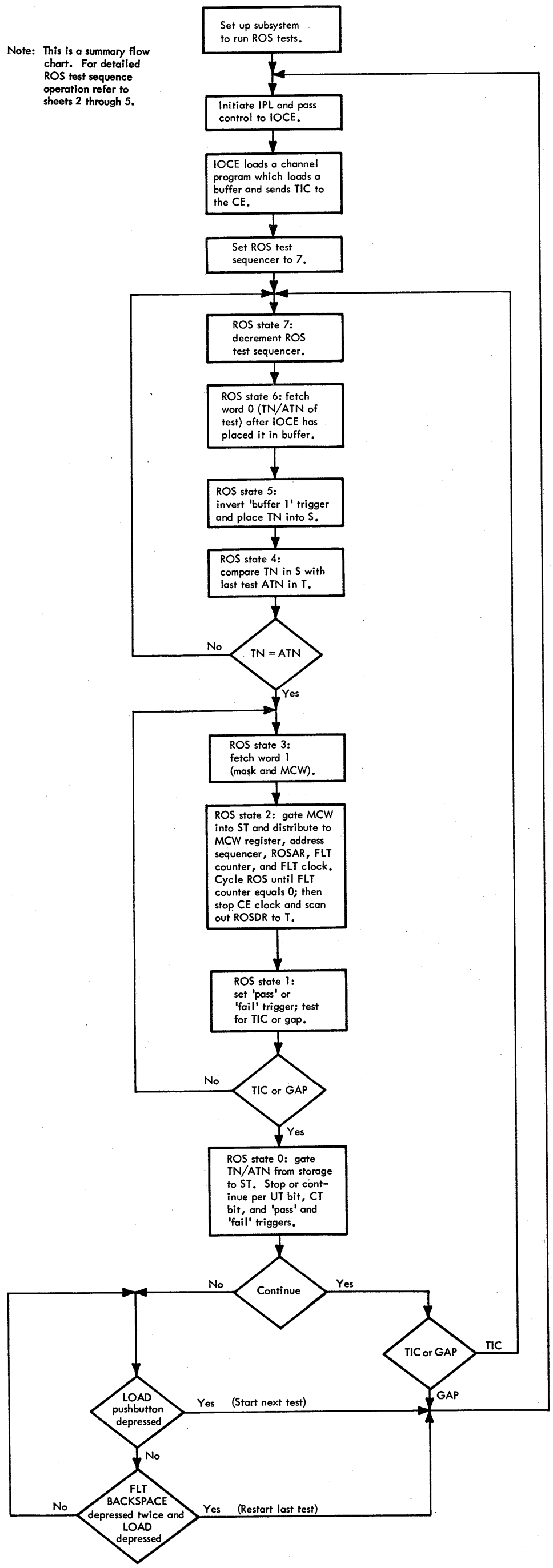


Diagram 6-115. ROS Test Sequence (Sheet 1 of 5)

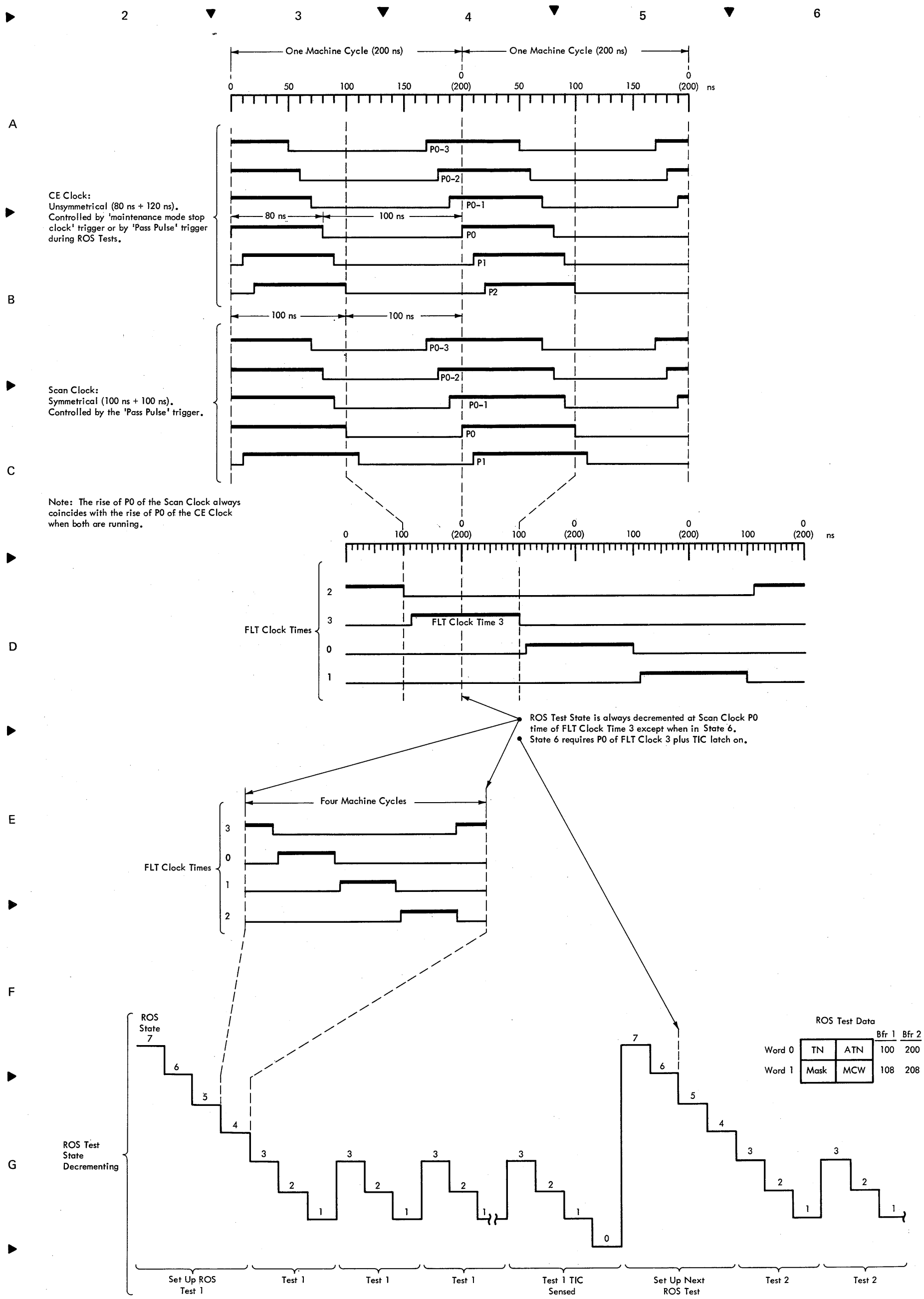


Diagram 6-115. ROS Test Sequence (Sheet 2 of 5)

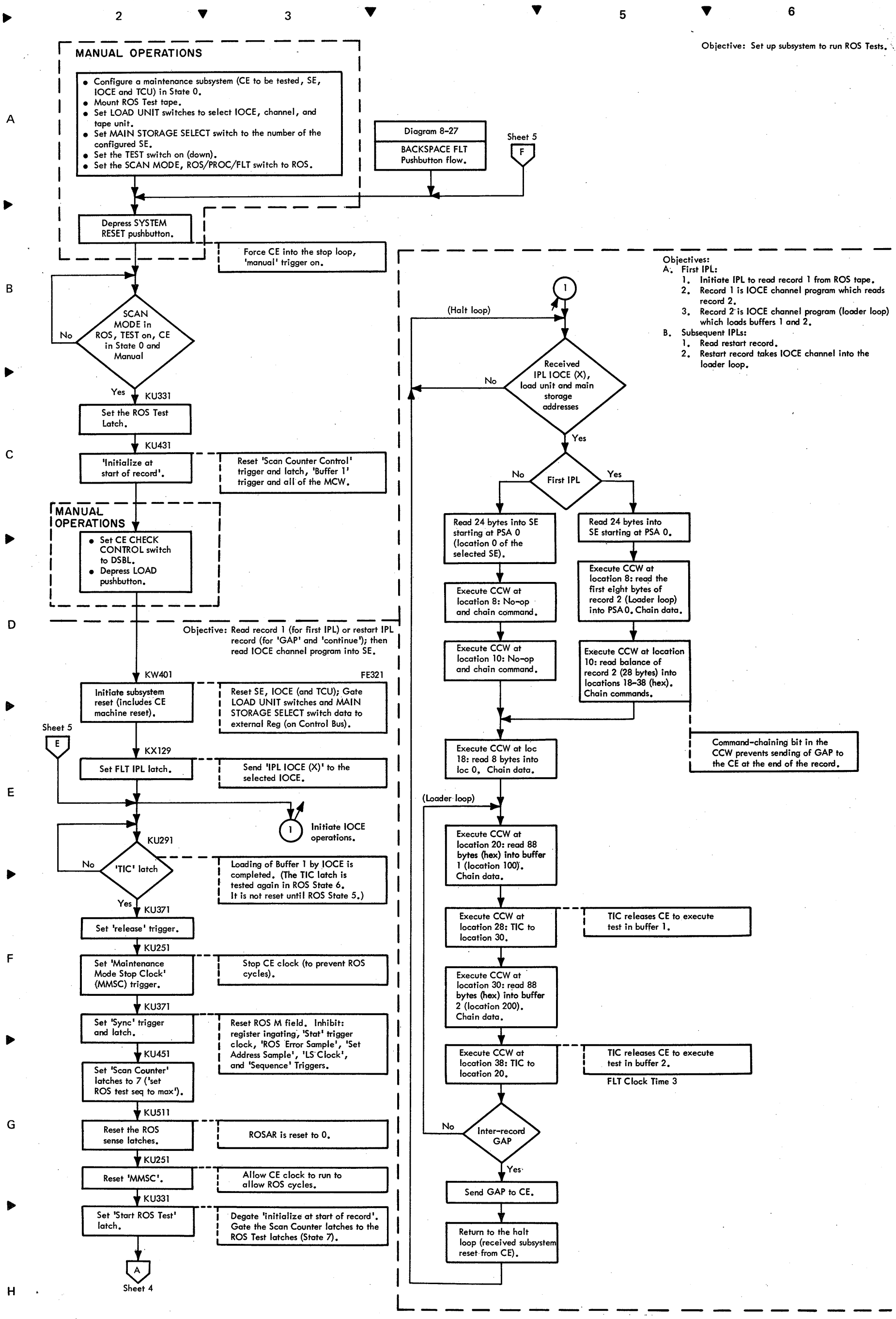


Diagram 6-115. ROS Test Sequence (Sheet 3 of 5)

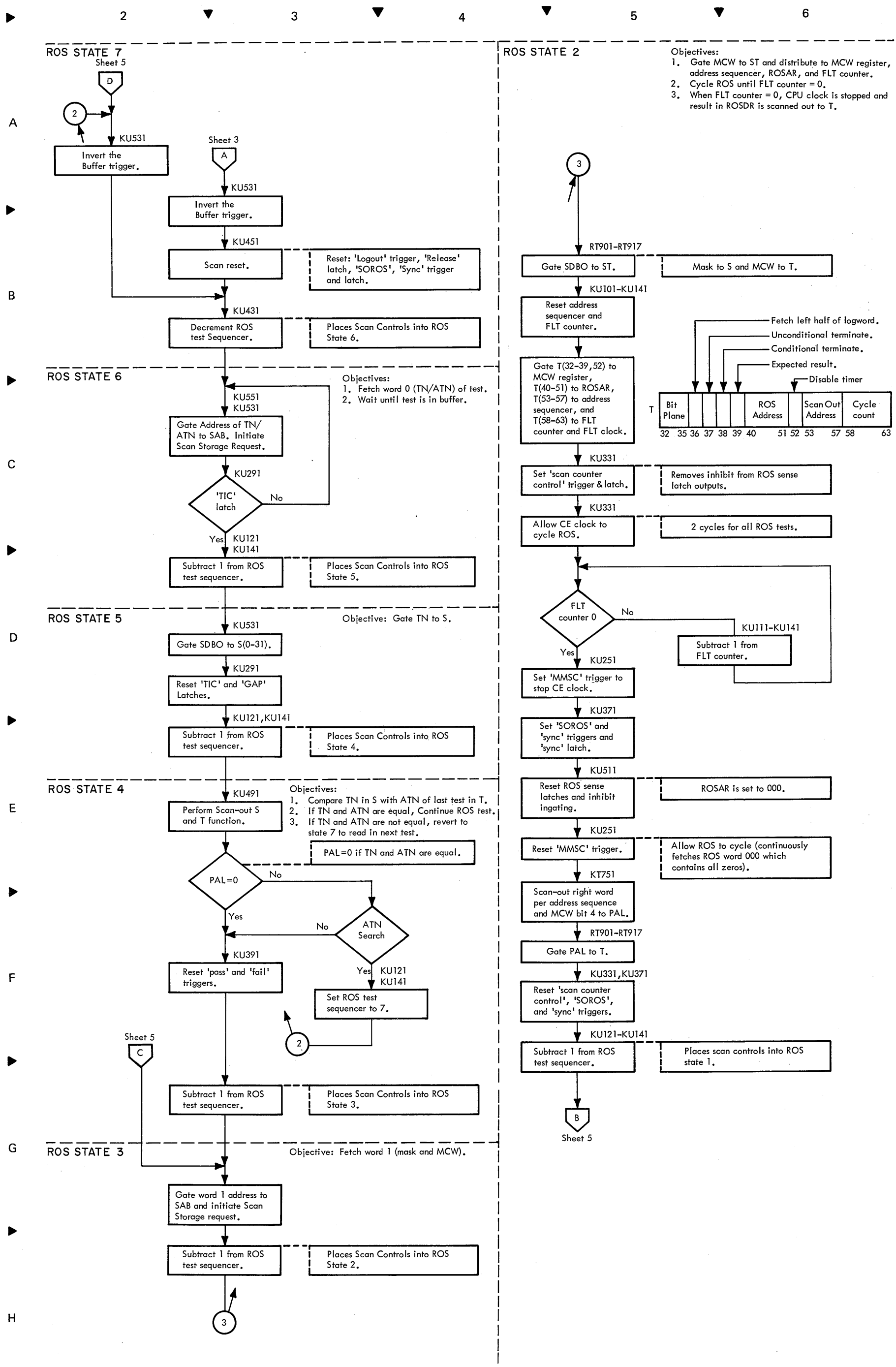


Diagram 6-115. ROS Test Sequence (Sheet 4 of 5)

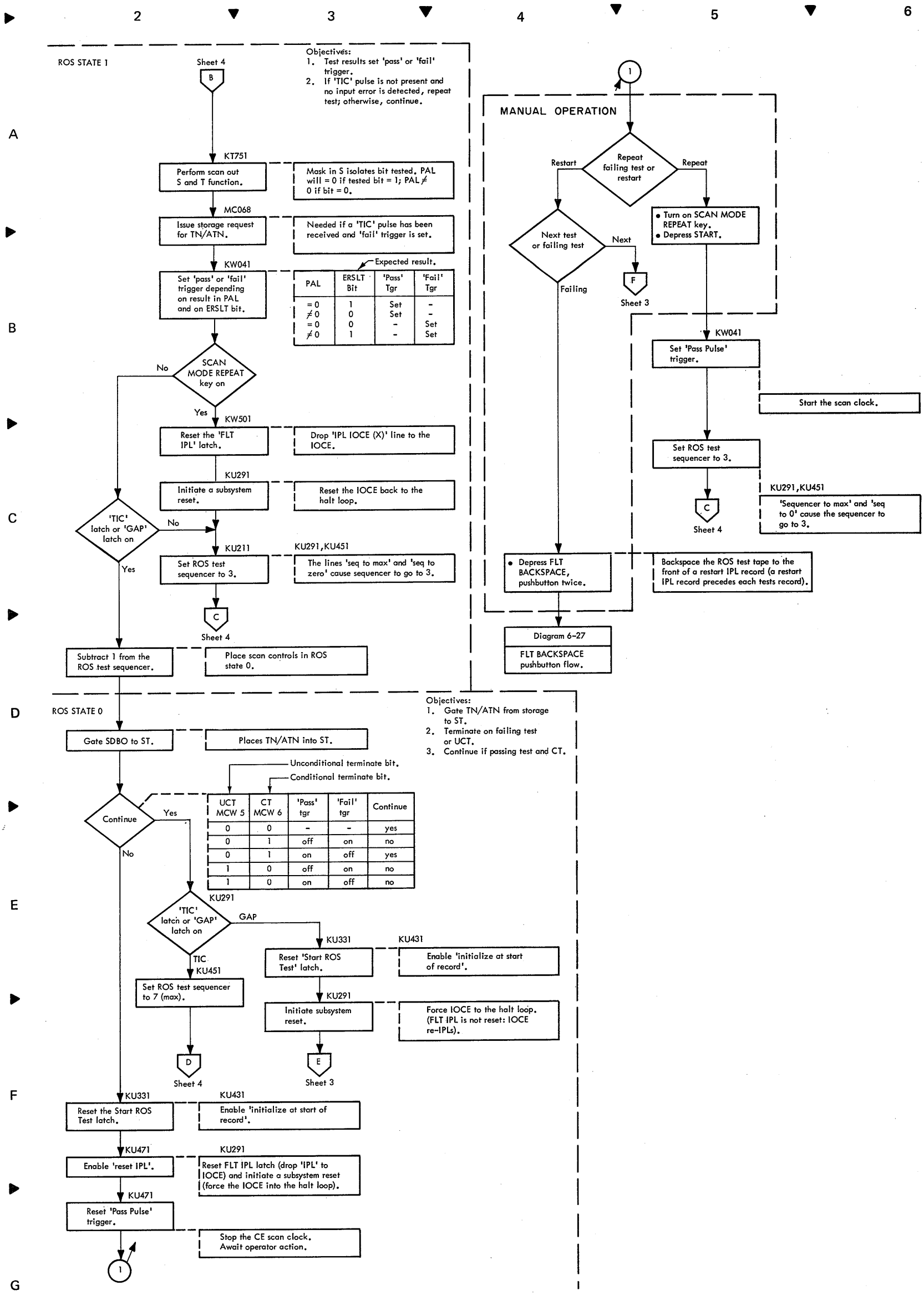


Diagram 6-115. ROS Test Sequence (Sheet 5 of 5)

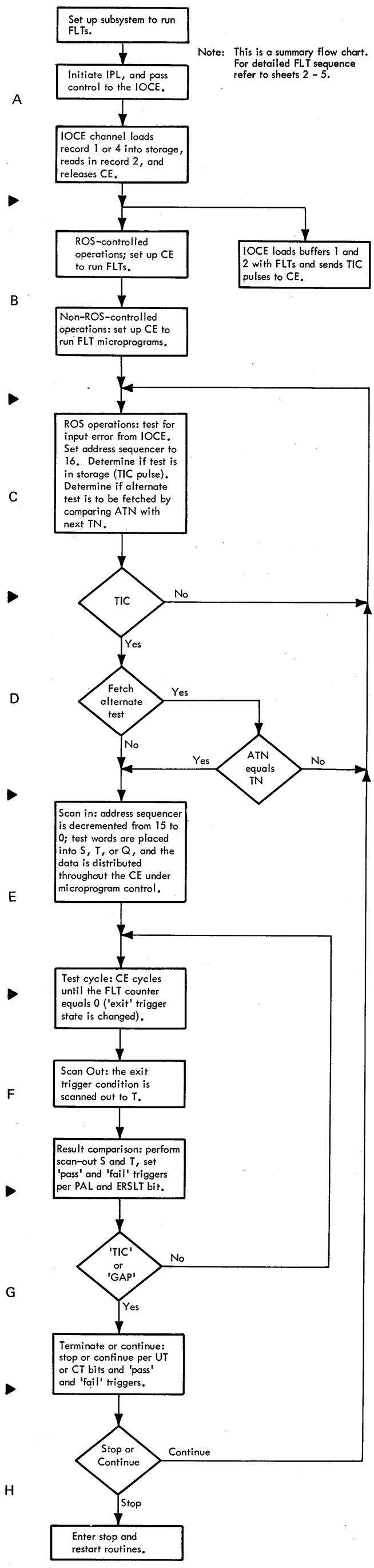


Diagram 6-116. FLT Sequence (Sheet 1 of 5)

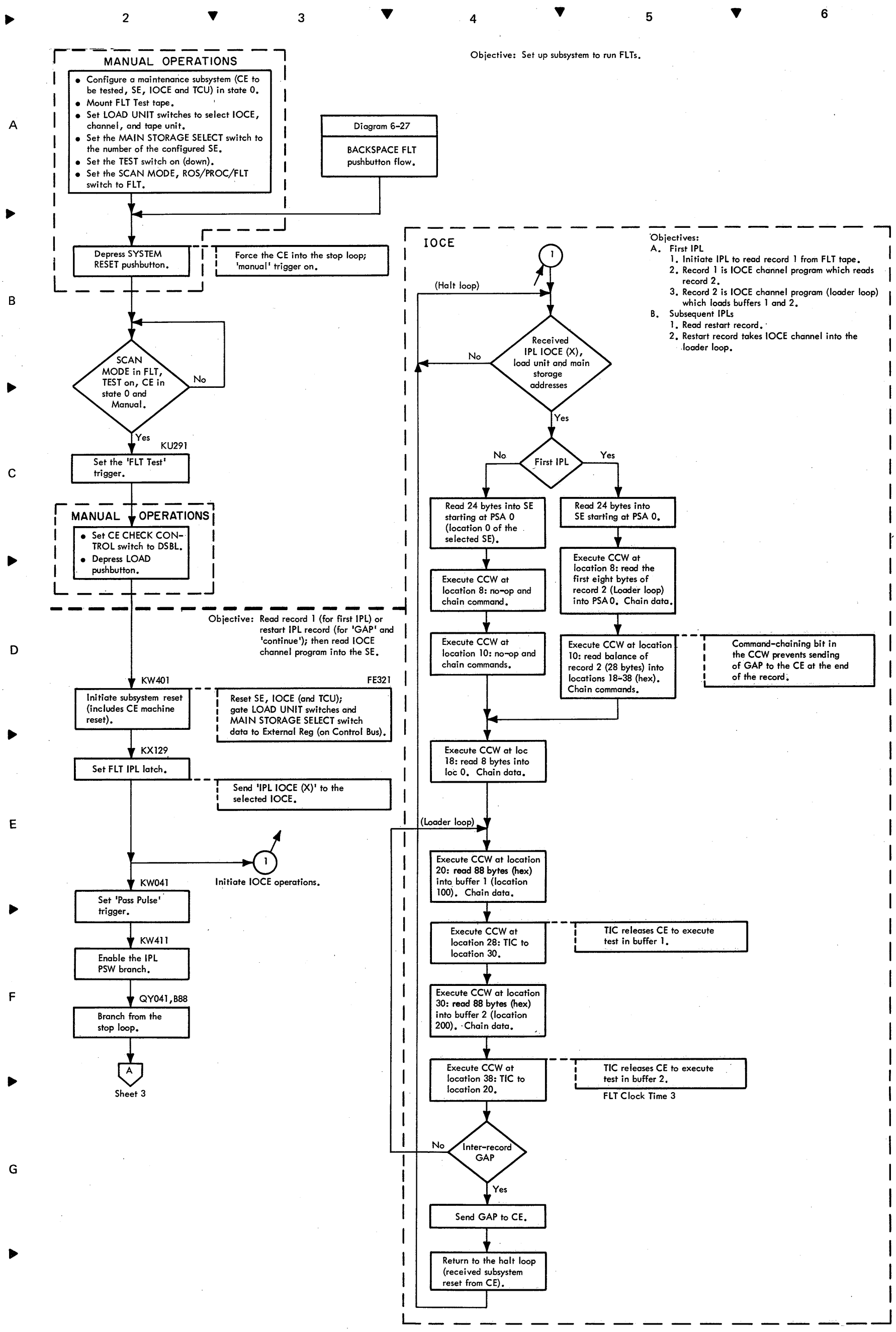


Diagram 6-116. FLT Sequence (Sheet 2 of 5)

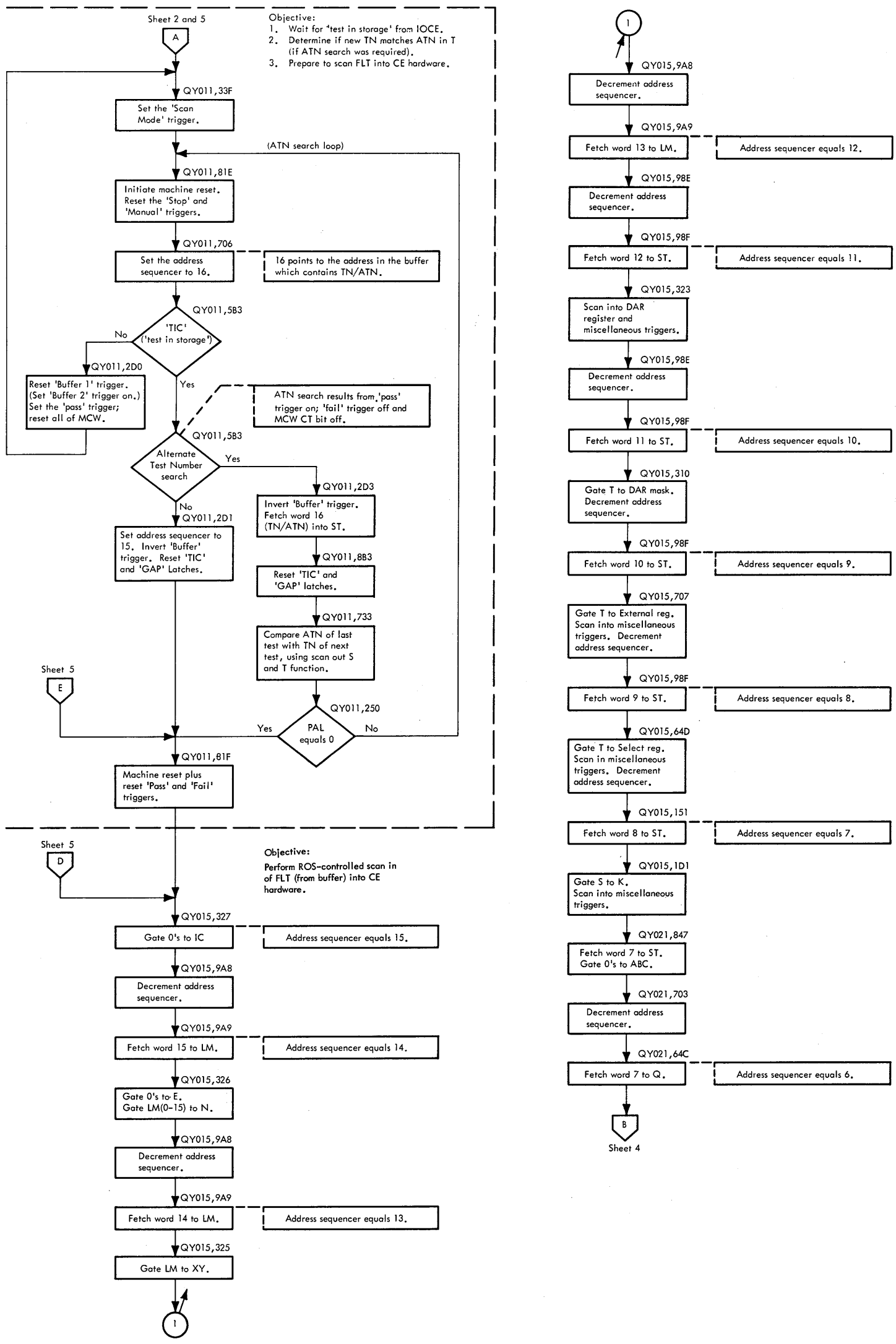


Diagram 6-116. FLT Sequence (Sheet 3 of 5)

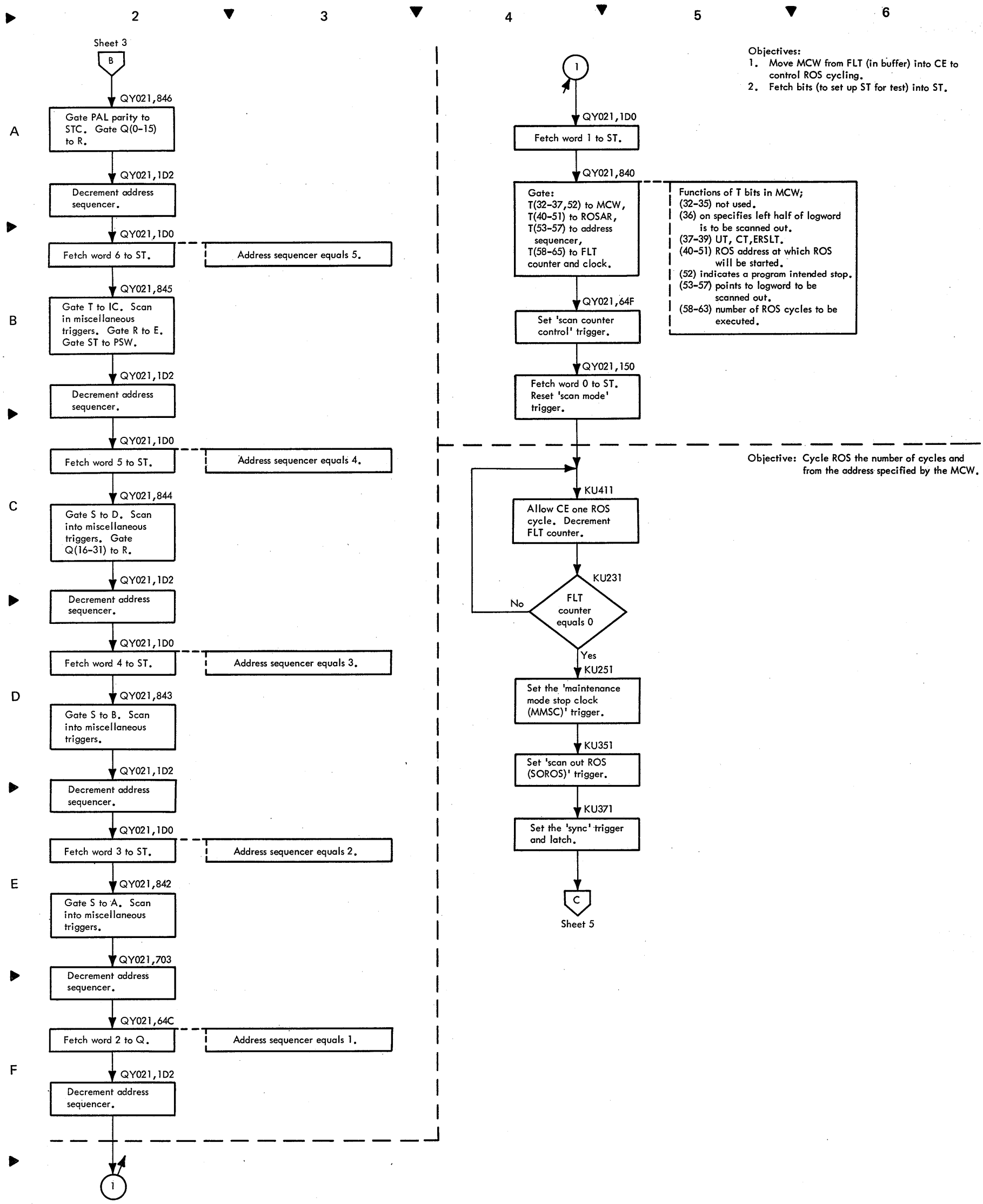
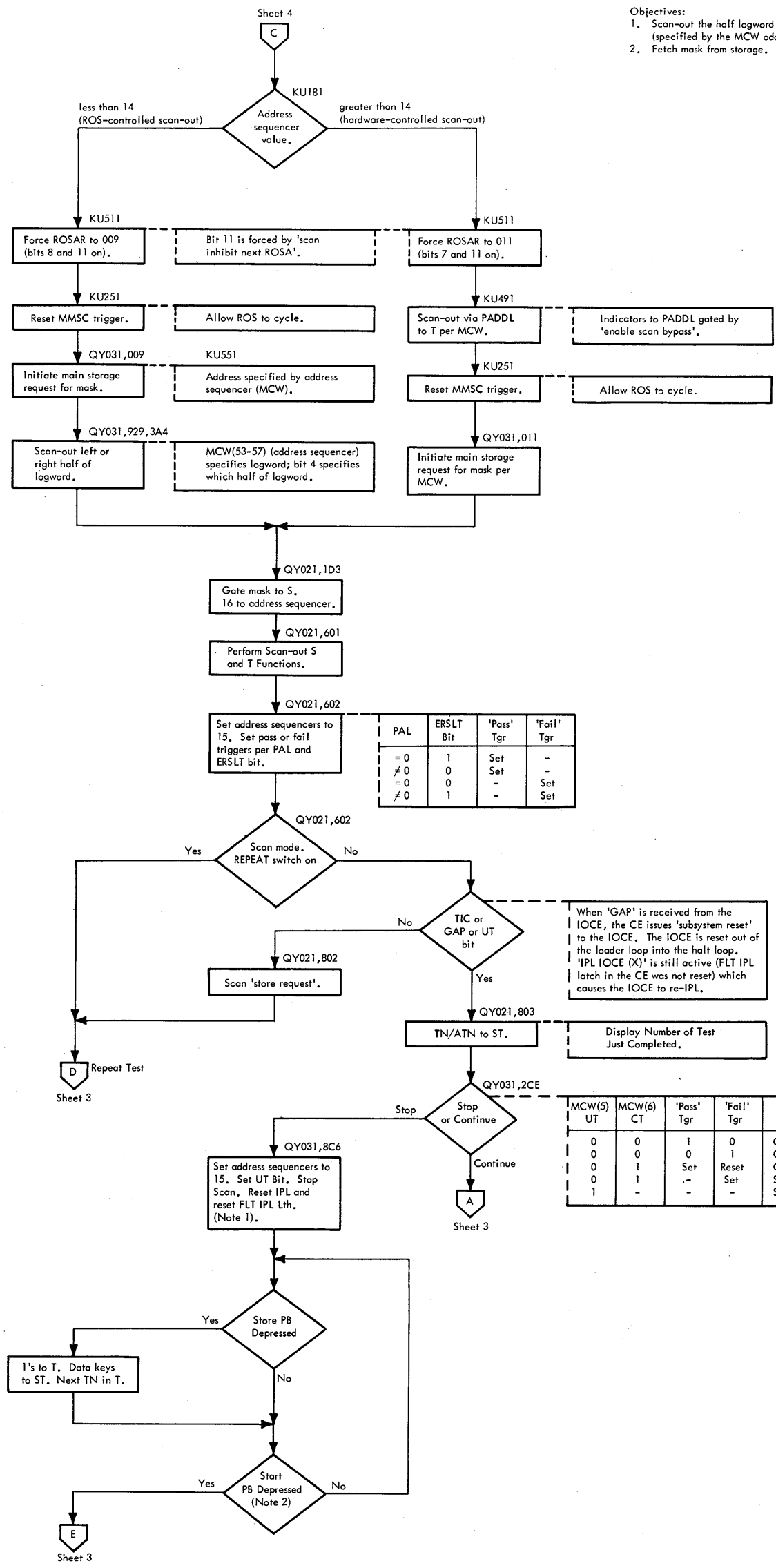


Diagram 6-116. FLT Sequence (Sheet 4 of 5)

Objectives:
1. Scan-out the half logword which includes the trigger being tested (specified by the MCW address sequencer).
2. Fetch mask from storage.



PAL	ERSLT Bit	'Pass' Tgr	'Fail' Tgr
= 0	1	Set	-
≠ 0	0	Set	-
= 0	0	-	Set
≠ 0	1	-	Set

MCW(5) UT	MCW(6) CT	'Pass' Tgr	'Fail' Tgr	Action
0	0	1	0	Continue (ATN Search)
0	0	0	1	Continue (next test)
0	1	Set	Reset	Continue (next test)
0	1	-	Set	Stop
1	-	-	-	Stop

Notes:
1. To restart after a stop, depress FLT BACKSPACE twice, then the LOAD Pushbutton once. This will bring in the next test and run it (Diagram 6-27).
2. To loop on failing test, operator must place SCAN MODE REPEAT Switch down before depressing START pushbutton.

Diagram 6-116. FLT Sequence (Sheet 5 of 5)

	LOG WORD NO.	PSA LOC-ATION	PSA WORD NO.	BIT POSITIONS IN MAIN STORAGE 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	COMMENTS
A	0	128 (80)	32	F REG P 0-7	D REG P 8-15	P 16-23	P 24-31					Q REGISTER P 0-7	P 8-15	P 16-23	P 24-31	P 32-39	P 40-47	P 48-55	P 56-63	DAR MASK P 0-7	P 8-15	P 16-23	P 24-31													PARITY FOR F, D, Q AND DAR MASK
		132	33	SELECT REG P 0-7	P 8-15	P 16-23	P 24-31					ST REGISTER P 0-7	P 8-15	P 16-23	P 24-31	P 32-39	P 40-47	P 48-55	P 56-63	CCR P 0-7	P 8-15	P 16-23	P 24-31													PARITY FOR SR, K, ST AND CCR
	1	136 (88)	34	CE SEL SATR 1		G REG P 0-7	P 32-39	P 0-7	ATR P 8-15	P 16-23	P 24-31	IC REQ	RPT INSTR ADJ	INSTR STEP TGR	DISABLE INTER-LEAVE	STAT TGR A	I FETCH 1 TGR	IL NOT AVAIL	EXT INTRPT CE4 WDD 28	MCW RTP 0	ADDR SEQ 0	FLT CLOCK 0		MARK P 0-7	ST REG P 32-39	AB REG P 64-67	PADDL P 64-67									
		140	35	EXTERNAL TRIGGERS PERMIT IOCE 2	3	LOGOUT IOCE 1	2	3				AB REGISTER P 0-7	P 8-15	P 16-23	P 24-31	P 32-39	P 40-47	P 48-55	P 56-63	R REG P 0-7	P 8-15	E REG P 0-7	P 8-15													
B	2	144 (90)	36	CE SEL SATR 2	3	4	TIME CLOCK STEP		SELECT IOCE 1	2	3	IOCE MC REQ	INTRPT GATE TGR			EXTERNAL REG P 0-7	P 8-15	P 16-23	P 24-31	G REG (WRITE DIRECT) 0	1	2	3	4	5	6	7	ATR-2 32	33	34	35	36	37	38	39	G REG, ATR-2
		148	37	PAM/RCU 1/1	2/2	3/	1	2	3	6	7	SELECT REGISTER SE/DE 1/	2/	3/	4/	5/	6/1	7/2	8/3	9/4	10/5	18	19	CE 1	2	3	4	24	25	26	27	28	IOCE 1	2	3	SELECT REG
C	3	152 (98)	38	ADDRESS TRANSLATION REGISTER (ATR-1) 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	ATR-1
		156	39	STAT TRIGGERS B	C	D	E	F	G	H	BLOCK I FETCH	I FETCH 2 TGR	I FETCH 3 TGR	EXEC IN PROG TGR		PROG STORE COMP	I FETCH REQ TGR	BR INV ADDR TGR	I FETCH INV ADDR TGR	CE1 WDD 20	CE1 RDD 21	CE2 WDD 22	CE2 RDD 23	EXTERNAL INTERRUPT REGISTER TIMER 24	PB 25	CE3 WDD 26	CE3 RDD 27	CE4 RDD 29	PIR 30	DAR 31	PIR 1	2	3		TIMING GT TGR	
	4	160 (A0)	40	PROGRAM STATUS WORD SYSTEM MASK 0	1	2	3	4	5	6	7	KEY 8	9	10	11	A 12	M 13	W 14	P 15	IC IN LSWR	COND CODE 34	35	PROGRAM STATUS WORD PROGRAM MASK 36	37	38	39	MC INTRPT		PROGRAM INTERRUPT CODE 8	4	2	1	INTERRUPT PRIORITY 1	2	PSW
		164	41	D REQ	SCAN REQ	SET KEY	INSERT KEY	3 CYCLE REQ	PAGE 1 LTH			RPT INSTR INIT	PULSE MODE ADJ	PULSE MODE INIT	STOP TGR	BLOCK TGR	PASS PULSE TGR	BLOCK INTRPT	FORCE ADDR TGR	SINGLE CYCLE TGR	CHECK SUM	CLOCK INHIBIT	RPT TEST	FLT TEST	ROS TEST TGR	SCC TGR	SYNC TGR	DISABLE INTER-LEAVE REV STOR ADDR	FLT BKSP	CONSOLE LOG OUT	SOROS	DIAG TGR	FLT REL	TIC	GAP	
D	5	168 (A8)	42	STORAGE CHECK ADDRESS REGISTER 0	1	2	3	360 MODE	TEST MODE	SE STPD IN 360 MODE		SAB CHK	SDBI CHK	SE/DE T/O	SE/DE ADDR CHK	SE/DE DATA CHK	CHECK REGISTER 2 FETCH CHK	LOS TO SE/DE		IOCE BUS CHK	LOCAL STORE BUS CHK	CCR PTY CHK	ATR PTY CHK	PSBAR PTY CHK	PSBAR NOT CONF	PSBAR ALT CHK	SPLIT LOG OUT	LOG ROS CHK	LOG ADDR CHK	CE LOG REQ	RDD T/O					CR2
		172	43	LACMP 1	RSA FSP 2	RMP 3	MCW REGISTER RSARP 4	5	LOC 6	7	DT 20	SCAN ADDRESS SEQUENCER 1	2	3	4	SCAN CYCLE COUNTER 0	1	2	3	FLT CLOCK 1		ROS TEST SEQUENCER 0	1	2					FLT PASS	FLT FAIL		FLT STG ERR		MAINT MODE STOP CLOCK	SCAN BUFFER 1	
	6	176 (B0)	44	EXTERNAL REGISTER 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	EXTERNAL REG
		180	45	MARKS 0	1	2	3	4	5	6	7								TX TGR	AB REG 64	65	66	67		ABC 0	1	2	PADDL 64	65	66	67	INSERT LOCAL STORE SIGN	STC 0	1	2	
E	7	184 (B8)	46	AB REGISTER 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	AB REG (0-31)
		188	47	AB REGISTER 32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	AB REG (32-63)

Diagram 6-117. CE Logword Formats (Sheet 1 of 3)

LOG WORD NO.	PSA LOC-ATION	PSA WORD NO.	BIT POSITIONS IN MAIN STORAGE																																COMMENTS
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
8	192 (C0)	48	PHYSICAL PSBAR 9	10	11	12	P 9-12	PSBAR COUNTER 9	10	11	P 9-15	9	10	11	12	LOGICAL PSBAR 13	14	15	16	17	18	19	ALT PSBAR				PROGRAM STATUS WORD D SYSTEM MASK 16	17	18	19	SE STPD 24	PSA LOCKOUT 1 25	2 26	3 27	PSBAR
	196	49	STATE S_0	S_1	SCON 1	2	3	4	ILOS 6		1/	2/	3/	4/	5/	CONFIGURATION CONTROL REGISTER (CCR) SE/DE 6/1	7/2	8/3	9/4	10/5	18	19	1	CE 2	3	4	24	25	26	27	28	IOCE 1	2	3	CCR
10	200 (C8)	50	1	SPARE	IOCE 2	SPARE	3	SPARE	1/	2/	3/	4/	5/	SE/DE 6/1	7/2	DIAGNOSE ACCESSIBLE REGISTER MASK 8/3	9/4	10/5	SPARE 16	SPARE 17	1/1	PAM/RCU 2/2	3/	1	TCU 2	3	CE OWN OTC	OBS	SPARE 26	1	CE 2	3	4	SPARE 31	DAR MASK
	204	51	SERIAL ADDER LATCHES (SADDL) 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	SADDL, IC
11	208 (D0)	52	R REGISTER 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	E REGISTER 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	R REG, E REG
	212	53	F REGISTER (READ DIRECT) 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	D REGISTER 16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	D REG, F REG
	216 (D8)	54	Q REGISTER 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Q REG
	220	55	Q REGISTER 32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	Q REG
12	224 (E0)	56	IOCE1 A	B	IOCE2 A	B	IOCE3 A	B	1/	2/	3/	4/	5/	SE/DE ELC 6/1	7/2	DIAGNOSE ACCESSIBLE REGISTER (DAR) 8/3	9/4	10/5	SPARE 16	SPARE 17	1/1	PAM/RCU ELC 2/2	3/	1	TCU ELC 2	3	CE OWN OTC	OBS	SPARE 26	1	CE ELC 2	3	4	SPARE 31	DAR
	228	57	PARALLEL ADDER FULL SUM-CHECK 4-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63									CHECK REGISTER 1 4-7	8-15	16-23	PARALLEL ADDER HALF-SUM CHECK 24-31	32-39	40-47	48-55	56-67				2-42	ROS PARITY CHECK 43-68	69-99	SADD HALF SUM CHK	SADD FULL SUM CHK	CR1
13	232 (E8)	58	LSWR P 0-7	P 8-15	P 16-23	P 24-31	E REG PTY 0-7	CHECK REG 1 PADD FULL SUM 64-67	MPR DECODE PTY CHK	PADD HALF SUM CHK	EXT TGRS PERMIT IOCE 1	IOCE INTRPT REQ	N REG P 0-7	P 8-15	PSW REG P 0-7	P 8-15	NO RETRY	SVC INTRPT	PHYS PSBAR PTY 9-12	PSBAR CNTR 12	LOGICAL PSBAR PTY 16-19		SADDL P 0-7	IC REG P 8-15	P 16-23	P 24-31									
	236	59	LOCAL STORAGE WORKING REGISTER (LSWR) 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	LSWR
14	240 (F0)	60																																	
	244	61	T32-63 TO PADDA 32-63	32-63 COMP	31-62 L1	31-62 C-L1	T 32-47 TO PADDA 48-63	T 48-63 TO PADDA 48-63	K 0-31 TO PADDA 32-63	D8-31 TO PADDA 8-31	7-30 L1	7-30 C-L1	40-63	40-63 COMP	FMTO	FMTM	FMTW	IC 8-31 TO PADDB 40-63	AB 4-7 TO PADDB 4-7	AB 8-31 TO PADDB 8-31	AB 32-63 TO PADDB 32-63	AB 64-67 TO PADDB 64-67	AB 6-31 TO PADDB 4-29L2	AB 32-67 TO PADDB 30-65L2	AB 64-67 TO PADDB 28-31	EX 6 TO PADDB 28-63	HOT ONE TO PADDB 60	E 8-11 TO PADDB 56-59	E 12-15 TO PADDB 60-63	E 8-11 TO PADDB 60-63	Q 4-15 TO PADDB 52-63	Q 20-31 TO PADDB 52-63	Q 36-47 TO PADDB 52-63	Q 52-63 TO PADDB 52-63	
15	248 (F8)	62																																	
	252	63	READ ONLY STORAGE DATA REGISTER (ROSDR) 70	71	72	73	74	75	76	77	79	80	81	82	83	84	P 43-68	86	88	89	90	P 69-99	92	93	94	95	97	98	99		RIGHT DIGIT TGR	S TGR	LEAVE TGR	STEP ABC TGR	ROSDR

Diagram 6-117. CE Logword Formats (Sheet 2 of 3)

	LOG WORD NO.	PSA LOC-ATION	PSA WORD NO.	BIT POSITIONS IN MAIN STORAGE	COMMENTS
A	16	256 (100)	64		
		260	65	READ ONLY STORAGE DATA REGISTER (ROSDR): 37, 38, 39, 40, 41, 42, 43, 44, 46, 47, 48, 49, 50, 51, 52, 53, 55, 56, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, INHIBIT LS WRITE, PROSA A LAST, FLT MODE	ROSDR
	17	264 (108)	66		
		268	67	READ ONLY STORAGE DATA REGISTER (ROSDR): 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 19, P 2-42, 21, 22, 23, 24, 25, 26, 28, 29, 30, 31, 32, 33, 34, 35	ROSDR
B	18	272 (110)	68	L REG: P 0-7, P 8-15, P 16-23, P 24-31; K REG: P 0-7, P 8-15, P 16-23, P 24-31	
		276	69	READ ONLY STORAGE ADDRESS REGISTER (ROSAR): 1, 2, 3, 4, 5, 6, 7, 8, 10, 11; PREVIOUS ROS ADDRESS (A): 0, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11; PREVIOUS ROS ADDRESS (B): 0, 1, 2, 4, 5, 6, 7, 8, 9, 10, 11	ROSAR, PROSA, PROSB
	19	280 (118)	70	M REG: P 32-39, P 40-47, P 48-55, P 56-63; X REG: P 0-7, P 8-15, P 16-23, P 24-31; Y REG: P 32-39, P 40-47, P 48-55, P 56-63; N REGISTER: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	N REG
		284	71	ROSAR: 0, 9; PROSA: A6, B3; READ ONLY STORAGE DATA REGISTER (ROSDR): 0, 9, 18, 27, 36, 45, 54, 63, 69, 78, 87, 96; S 0-31 TO PADDA 32-63; D 8-31 TO PADDA 8-31 C; AB 0-31 TO PADDB 32-63; F 4-7 TO PADDB 60-63; LOCAL STORAGE ADDRESS REG: 0, 1, 2, 3, 4; WR LOCAL STORE	ROSAR, LSAR
C	20	288 (120)	72	K REGISTER: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	K REG
		292	73	MAINTENANCE CONTROL WORD (MCW): DE/SE 32, 33; SELECT 34, 35; DG SELECT 36, 37, 38, 39; CVG SELECT 40, 41, 42, 43; 44, 45; RNOP 46; FDGR 47; DSE 1 48; RERP 49; RC 50; WRAP DE 51	MCW
	21	296 (128)	74	LM REGISTER: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	LM REG
		300	75	LM REGISTER: 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63	LM REG
D	22	304 (130)	76	XY REGISTER: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	XY REG
		308	77	XY REGISTER: 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63	XY REG
	23	312 (138)	78	ST REGISTER: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	ST REG
		316	79	ST REGISTER: 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63	ST REG

Diagram 6-117. CE Logword Formats (Sheet 3 of 3)

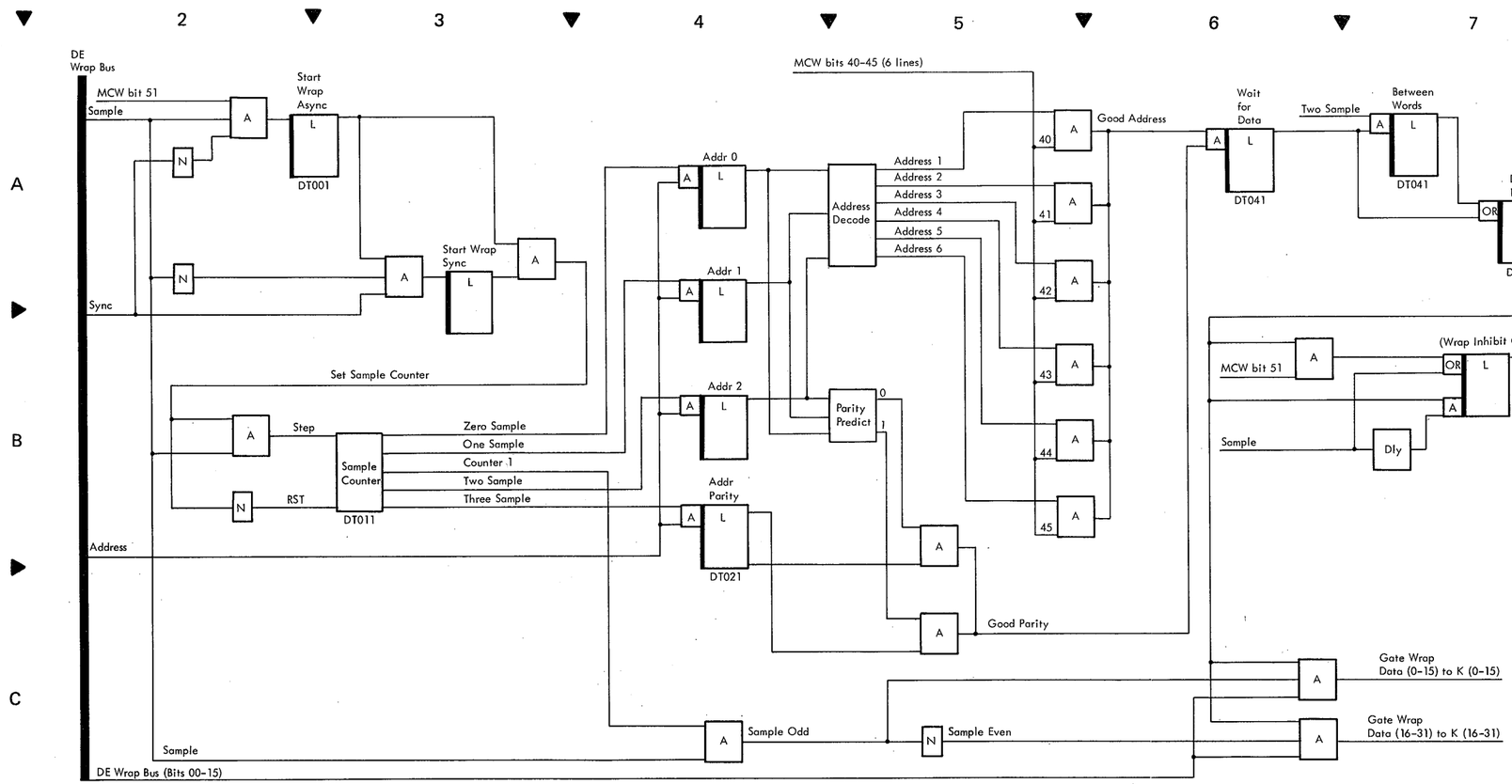
E

WORD NO.	BIT POSITIONS IN MAIN STORAGE 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	COMMENTS
0	SESDR (EVEN) (or IOCE SBO)																																SESDR (EVEN)
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
1	SESDR (EVEN)																																SESDR (EVEN)
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	
2	MARKS (EVEN)									IOCE SAB (EVEN)																							MARKS, SESAR (EVEN)
	0-7	8-15	16-23	24-31	32-39	40-47	48-53	54-63		TAG (EVEN) 1	2	3	4	HI/LO 5	SESAR 1-14 (EVEN) 6	7	8	9	10	11	12	13	14	15	16	17	18	19	IOCE SAB 20	21	22	23	
3	CCR(0-7)								REQUEST (EVEN)								RESPONSE (EVEN)								CCR (8-15)								CCR, REQUEST AND RESPONSE LATCHES (EVEN)
	CE 1	2	3	4		IOCE 1	2	3	CE 1	2	3	4	IOCE 1	2	3		CE 1	2	3	4	IOCE 1	2	3		STATE S_0	S_1	SCON 1	2	3	4	14	15	
4										SE ID							OPERATION		OPERATION (EVEN)				BLK SEL LATCH		SCON BACK UP LATCHES				MARK PARITY (EVEN)	ADDR PARITY			TYPE OF OP (EVEN)
										1	2	3	4				ISK	SSK	T & S	STORE	FETCH	SUPP LOG CHK	EVEN	ODD	1	2	3	4		1-5 0-7	6-12 8-15	13-19 16-23	
5	CHECK CONDITION (EVEN)								CHECK CONDITIONS (COMMON)														CCR PARITY		SESDR PARITY (EVEN)								CHECKS (EVEN AND COMMON), SESDR (EVEN)
	MARK PARITY CHK	ADDR PARITY CHK	DATA PARITY CHK	SP PARITY CHK	KEY	NORMAL OP CHK			CCR	TAG PARITY CHK	TAG	SAB (IOCE)	SBO (IOCE)				OBS	OTC THERMAL					0-7	8-15	SBO (IOCE) 0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63	
6	SESDR (ODD)																																SESDR (ODD)
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
7	SESDR (ODD)																																SESDR (ODD)
	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	
8	MARKS (ODD)									IOCE SAB (ODD)																							MARKS, SESAR (ODD)
	0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63		TAG (ODD) 1	2	3	4	HI/LO 5	SESAR 1-14 (ODD) 6	7	8	9	10	11	12	13	14	15	16	17	18	19					
9									REQUEST (ODD)								RESPONSE (ODD)																REQUEST AND RESPONSE LATCHES (ODD)
									CE 1	2	3	4	IOCE 1	2	3		CE 1	2	3	4	IOCE 1	2	3										
10	SPIKR								SPOKR										OPERATION (ODD)										MARK PARITY (ODD)	ADDR PARITY			SPIKR, SPOKR, TYPE OF OP (ODD)
	P 0-4	0	1	2	3	4			P 0-4	0	1	2	3	4					T & S	STORE	FETCH	SUPP LOG CHK								1-5 0-7	6-12 8-15	13-19 16-23	
11	CHECK CONDITION (ODD)						SPAR																		SESDR PARITY (ODD)								CHECKS (ODD), SPAR, SESDR (ODD)
	MARK PARITY CHK	ADDR PARITY CHK	DATA PARITY CHK	SP PARITY CHK	KEY	NORMAL OP CHK	P	X	Y	2	3	4	5	6	7										0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63	

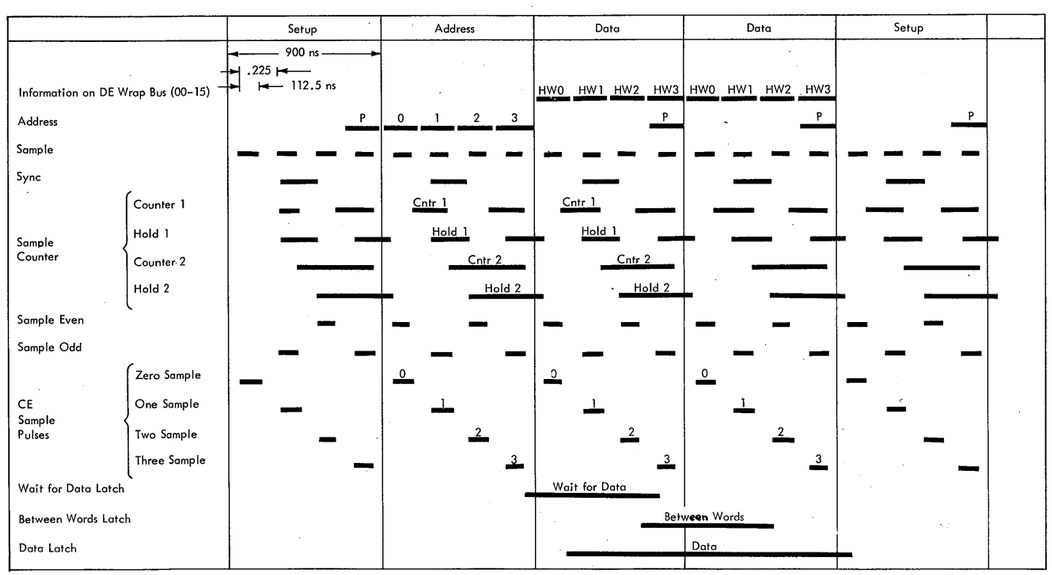
Diagram 6-118. SE Logword Formats

	WORD NO.	BIT POSITIONS IN MAIN STORAGE																																COMMENTS
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
A	0	DESDR (EVEN)																																DESDR (EVEN)
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
	1	DESDR (EVEN)																																DESDR (EVEN)
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	
	2	MARKS (EVEN)								DESDR PARITY (EVEN)								DESAR 1-14 (EVEN)																MARKS DESDR, DESAR (EVEN)
		0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63	0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63	P 6-12	6	7	8	9	10	11	12	P 13-19	13	14	15	16	17	18	19	
B	3	MARK PARITY	T & S	STORE	FETCH	DATA CHK	ADDR CHK	MARK PARITY CHK	CANCEL LATCH			SPIKR						SPOKR						OPERATION		CHECK CONDITION (COMMON)								CHECKS (EVEN AND COMMON), SPIKE, SPOKE
												P 0-4	0	1	2	3	4	P 0-4	0	1	2	3	4	ISK	SK	SP ADDR CHK	SP KEY CHK	KEY MIS-MATCH	OBS	OTC				
	4	DESDR (ODD)																																DESDR (ODD)
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
	5	DESDR (ODD)																																DESDR (EVEN)
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	
	6	MARKS (ODD)								DESDR PARITY (ODD)								DESAR 1-14 (ODD)																MARKS DESDR, DESAR (ODD)
		0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63	0-7	8-15	16-23	24-31	32-39	40-47	48-55	56-63	P 6-12	6	7	8	9	10	11	12	P 13-19	13	14	15	16	17	18	19	
C	7	MARK PARITY	T & S	STORE	FETCH	DATA CHK	ADDR CHK	MARK PARITY CHK	CANCEL LATCH																									CHECKS (ODD)
	8	CCR																																CCR
		DG																				STATE		SCON						CE				
		P 0-7	1A	1B	2B	2C	3C	3D	4D	4A	P 8-15	5A	5B	6B	6C	7C	7D	8D	8A	P 16-23	S_0	S_1	1	2	3	4	IDES		1	2	3	4	CCR INVALID	
	9	RESPONSE																																RESPONSE LATCHES, DG ADDR REG ID
		CE				A						B				CVG		C						D						ADDRESS REG			
		1	2	3	4	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	A	B	C	D	
	10	DG REGISTER CHECK								CHECK CONDITIONS (COMMON)								DG ADDRESS REGISTER																CHECKS DG ADDR REG
		1	2	3	4	5	6	7	8	TAG PARITY CHK	TAG	CCR PARITY CHK	MULTI ACCEPT	LS PARITY CHECK	NORMAL OP	REFRESH PARITY CHECK		P 1-7	1	2	3	4	5	6	7	P 8-14	8	9	10	11	12	13	14	
D	11	TAG						DE ID				HALFWORD COUNTER				DG DATA REGISTER																		DG DATA REG
		P 1-5	1	2	3	4	5	1	2	3	4	8	4	2	1	P 0-7	0	1	2	3	4	5	6	7	8-15	8	9	10	11	12	13	14	15	

Diagram 6-119. DE Logword Formats



* The output of this latch stops the CE clock to compensate for the difference in timing between the CE clock and the sample pulses received from the DE. One CE clock cycle is 200 ns while one sample pulse is 225 ns. Note that the CE clock is not allowed to run until the Data Latch turns on.



Note:
The chart at the left shows the timing for transferring one quadword of data to the CE via the DE Wrap Bus. The Diagnose instruction controls the total number transferred by setting the quadword count in the MCW.

A-Register (see AB-Register)
AB-Register:
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Divide, Fixed-Point 5-110 (Sheet 4)
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Add, A (5A); Fix Pt, RX 5-108
Add, AP (FA); Dec, SS:
Complement Add Sequence 5-303
GIS 5-301
True Add Sequence 5-302
Add, AR (1A); Fix Pt, RR 5-108
Add Halfword, AH (4A); Fix Pt, RX 5-108
Add Logical, AL (5E); Fix Pt, RX 5-108
Add Logical, ALR (1E); Fix Pt, RR 5-108
Add Normalized, AD (6A); Fl Pt, RX (Long) 5-207
Add Normalized, ADR (2A); Fl Pt, RR (Long) 5-207
Add Normalized, AE (7A); Fl Pt, RX (Short) 5-206
Add Normalized, AER (3A); Fl Pt, RR (Short) 5-206
Add Unnormalized, AU (7E); Fl Pt, RX (Short) 5-206
Add Unnormalized, AUR (3E); Fl Pt, RR (Short) 5-206
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Branch on Count, BCT (46); RX 5-504
Branch on Count, BCTR (06); RR 5-504
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Add Logical, AL (5E); RX 5-108
Add Logical, ALR (1E); RR 5-108
Compare, C (59); RX 5-108
Compare, CR (19); RR 5-108
Compare Halfword, CH (49); RX 5-108
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